Single Pin Redundancy for Robust Power Grid Delivery

***Abstract*— C4 bumps are susceptible to electromigration failure due to large power-supply currents. Electromigration failure is exacerbated by manufacturing variability, which increases bump resistance and consequently the current draw in neighboring bumps. A typical solution entails adding redundant bumps while guard-banding the maximum current per bump. Instead, we propose a mixed-integer linear program for redundant bump placement that minimizes the total bump count, while ensuring power supply integrity in the presence of a single-bump failure (SBF). Our experiments show a power grid can be made resilient to SBF by adding 32% more bumps, compared to 77% used in a greedy approach.**

I. Introduction

Robust power delivery is an increasingly important task in modern integrated circuits (ICs) due to increasing power and power density. This power increase complicates power supply network (PSN) design due to static (IR) voltage drop, transient voltage droop, and electromigration current constraints.

The power in most modern ICs is supplied using flip-chip pins. Unfortunately, flip-chip assemblies are becoming more prone to yield issues due to the increase in pin count and the shift to no-flow underfill processes [5]. Specifically, no-flow underfill processes are susceptible to void formation, non-wetting of solders and chip floating [2]. A single power pin failure/defect can lead to voltage drop violations within the IC and electromigration violations in other pins.

In this work we present a method for redundant power pin placement such that the PSN is single-pin redundant meaning, if any one pin fails due to a manufacturing defect, the design will still meet both the electromigration and static/dynamic voltage constraints. The problem is formulated and solved as an Integer Linear Program. Our methodology is unique since all previous power pin placement algorithms [4], [6] have focused on generating an initial power pin placement set that meet all design constraints without considering the robustness of the pin placement to single pin failures/defects.

II. Single Pin Redundancy

The goal of single pin redundancy is to augment a power pin placement with a minimal pin set (R_p) such that for any single pin defect, the nearby pins will not suffer from a cascading electromigration failure and all nodes within the design will continue to satisfy minimum static and transient voltage constraints.

Generating R_p is accomplished by first determining which pins within the design are critical and need to be made redundant and then determining which redundant pin locations can provide coverage for these critical pins.

Calculating the critical pin set (C_p) is accomplished by repeatedly simulating the PSN and removing a different pin each simulation. During each simulation the current through each pin, and the static IR voltage drop of the PSN are checked to ensure that they do not violate any design constraints. If either of the design constraints are violated the pin that is removed is added to C_p.

Calculating the coverage of a redundant pin location is done using a distance base metric. Redundant pins placed within a certain distance (d_{cover}) of a pin from C_p will provide redundant coverage for that pin due to the locality effect [1]. The value of d_{cover} is empirically determined and depends on the resistivity of the grid, total current in the PSN and the number of pins in the PSN.

The redundancy pin set is generated using a ILP. Given the different pins from C_p that each redundant pin location can cover, the goal of the ILP is to select the smallest set of redundant pins such that every pin from C_p is covered. The experimental results on applying our algorithm to the IBM power grid benchmarks [3] are shown in Table I. The Naive column, represents the results when a greedy algorithm is used to select R_p from the possible redundant pin locations. The Trans. Viols row represents the average number of transient violations for any single pin failure, and the Em. Viols row specifies the total number of pins within the design that could have an electromigration failure due to any single pin defect/failure

TABLE I

Pin Redundancy Set Generation Results

	No Redundancy	Naive	ILP
Added Pins	0	77%	32 %
Trans. Viols	0.60%	0.00%	0.00%
Em. Viols	52%	0%	0%
Runtime	0	142.24	154.39

III. Summary

In this work we present an ILP formulation for generating a redundant power pin set to guarantee single pin redundancy. Our ILP formulation was able to generate redundant pin sets for the IBM power grid benchmarks using only 32% more additional pins on average.

References

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