Eric W. Savage

545 W. Hacienda Ave #308, Campbell, CA 95008; 831.345.5598
savage@alumni.cse.ucsc.edu - http://alumni.cse.ucsc.edu/~savage

OBJECTIVE: Software Engineer for CAD applications or embedded devices

EDUCATION: M.S., Computer Engineering, University of California, Santa Cruz, Graduated March 2000
B.S., Computer Engineering, University of California, Santa Cruz, Graduated June 1998
Highest Honors in the Major

EXPERIENCE:

6/05-PRESENT Software Engineer
Intel Corporation, Santa Clara Design Technology and Solutions Group

- Implemented features within an Automatic Test Pattern Generation (ATPG) tool for microprocessors and chips sets.
- Determined and clarified design team requirements prior to writing specifications for feature development.
- Maintained GNU autotools based build and specialized regression environments.
- Ported and validated C++ code through numerous compiler and platform changes.
- Projects included interactive debug, enhanced ATPG learning, and Design for Test (DFT) validation features through a programming interface.

4/00-6/05 CAD Engineer
Intel Corporation, Santa Clara Design Technology and Solutions Group

- Worked with a very small team to enable Defect Based Test. Responsibilities included:
  - Productized fault extraction, fault mapping, and fault sampling for several fabrication defect models.
  - Pioneered ATPG execution for several defect models and delivered those test patterns for production testing.
  - Developed and refined innovative methodologies to increase coverage metrics through controlled experiments.
- Evaluated microprocessor test patterns to identify test holes and help improve product yield. Responsibilities included:
  - Collected test pattern effectiveness through fault simulation on initial and subsequent patterns used to fill test holes.
  - Reported test patterm effectiveness to determine locations of test holes and track progress of subsequent tests.

7/99-9/99; 6/98-9/98 Graduate Intern Technical
Intel Corporation, Santa Clara Design Technology Group

- Implemented a tool from scratch in C++ that transforms data from a variety of VLSI layout formats. Used layouts from microprocessor functional blocks. Extracted data was passed to an Inductive Fault Analysis (IFA) tool.
- Developed capabilities that extracted layout information, connected polygons, and propagated electrical net name information within and across metal layers.

- Validated results and compared run times from industry standard tools.

10/96-7/99 Student Programmer
Computer Engineering Department, University of California, Santa Cruz

- Worked with a small group on an Inductive Fault Analysis (IFA) tool written in C to identify possible defect locations in VLSI CMOS circuits.
- Developed and released new features for the IFA tool.
- Resolved bugs and answered questions from customers.

6/96-9/96 Information Technologies Student Intern
Modesto Irrigation District, IT Department

- Designed and implemented the District's web page.
- Installed network clients and network client applications.
- Installed and upgraded new hardware and resolved software problems.

TOOLS:

C, C++, Perl, Tcl/Tk, shell scripting, autotools, UNIX, and a variety of assembly languages.

Limited scope of Python, Javascript, and AJAX.

PUBLICATIONS:

S. Chakravarty, Y. Chang, E.W. Savage, et al. Experimental Evaluation of Bridge Patterns for a High Performance Microprocessor VTS 2005, pp. 337-342, May 2005

S. Chakravarty, E.W. Savage, E.N. Tran Defect Coverage Analysis of Partitioned Testing ITC 2004, pp. 907-915, Oct 2004

S. Chakravarty, A. Jain, E.W. Savage, et al. Experimental Evaluation of Scan Tests for Bridges ITC 2002, pp. 509-518, Oct 2002

S. Chakravarty, K. Komeyli, E.W. Savage. et al. Layout Analysis to Extract Open Nets Caused by Systematic Failure Mechanisms VTS 2002, pp. 367-372, May 2002