Pranav Kumar Natesh

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SUMMARY A Graduate student pursuing MS in Computer Engineering. To leverage my experience in FPGA and ASIC development and to contribute meaningfully to my team with efficient/enhanced designs and project execution.

OBJECTIVE To have a full-time position leading to a career in Hardware Design and Verification.

EDUCATION

Masters of Science, Computer Engineering — Sep 2009 - Jan 2012 (Expected)
University of California, Santa Cruz
Concentration: Computer Architecture and Hardware Design

Bachelor of Technology, Electrical and Electronics — Sep 2005 - May 2009
SRM institute of Science and Technology, Chennai, India

RELEVANT COURSEWORK Advanced Microprocessor Design, Computer Architecture, Logic Design with Verilog, Graduate level Analysis of Algorithms, VLSI Digital System Design, Multimedia Systems, Micro-Controller based System Design, Microprocessor and Its Applications, Digital Systems, Linear Integrated Circuits, Electronic Circuits, Electrical Circuits, Three Courses in Engineering Mathematics

SKILLS

Software Skills: Verilog, System Verilog, System Verilog Assertions, C/C++, Python, Perl, TCL, UNIX, VI
Front End Tools: ModelSim, Synopsys VCS, Synplify Pro, Altera Quartus, NIOS IDE, Xilinx ISE Design suite, Synopsys DC, Verilog PLI
PCB Layout Tools: Cadence Allegro
Embedded Systems: Intel 8086 8051
Instruments: Oscilloscopes, Logic Analyzer, Function Generators, Multimeters

EMPLOYMENT

ASIC Design Intern — Oct 2011 - Present
Sandforce Inc. / LSI Logic

- Block-Level Functional Verification of a Subsystem
- FPGA Emulation : Synthesis and reporting scripts.
- Wrote Register Descriptions in RDL for certain key blocks.

Thesis Research — Mar 2010 - Present
Micro-Architecture Group(MASC) at University of California, Santa Cruz.

- Part of the team working on the SCOORE project (Santa Cruz out-of-order RISC Engine) under the supervision of Prof. Jose Renau.
- Design and Verification owner of the Floating Point Unit.
- Design of a Programmable Testing Unit for the FPU.
- The Floating Point Node is planned to be taped on the 28nm GF process, as a part of the MURN project.

Hardware Engineering Intern — July 2010 - Sep 2010
Juniper Networks (Enterprise Products Group)

- Performed Functional Verification and Modelling for the Ethernet Switch control board.
- Automated the FPGA build flow : RTL to bitstream.
- Performed Quality Analysis of various clock oscillator vendors.

PROJECTS

FPGA-based Video Image Capture System: Designed on an Altera Nios II System serving a client PC as a socket server.
VLSI Power Grid Analysis: The Random-Walk algorithm was used to achieve a better accuracy/run-time trade-off.
Nokia Application Development: Inbuilt Camera controlled Cursor.
FPGA Based FFT Spectrum Analyzer: Completed as a part of my undergraduate study at SRM University, gained experience with MATLAB system generator and AccelDSP.