**Frederick Kilner**

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**OBJECTIVE:**

Hardware bring up and testing. Write tests for manufacturing and support contract manufacturers. Program in C, C++, JAVA, Python, TCL/TK and BASH. Debug logic in Verilog. Use logic design tools such as Xilinx ISE/Vivado.

**12/2017, Completed a Python programming and Solidworks CAD class.**

**2017, Returned from over three months traveling around Europe, the UK and Israel.**

**2016, Xilinx Vivado, Xilinx SDK and Android Studio**

* I was beginning at a start up where I would do microblaze programming using Xilinx SDK but unfortunately the company fell through. I like using Verilog in Xilinx FPGAs.
* Started using Android Studio because previously I had written an unpolished space invaders game in Android and want to continue getting good at Android.

**5/2015-12/24/2015 , Completed ASIC Test Engineer Contract, Ericsson Silicon Valley, San Jose, CA**

* Modify and write TCL/Expect scripts to test ASICs on board running under Linux.
* Use Thermotron and Peltier for thermal testing.
* To test ASICs work with BGA sockets and deal with their and board issues.
* Use IXIA to run traffic. Run manually and modify scripts for various scenarios.

**2/2015-5/2015, Test Technician, Granite River Labs, Santa Clara, CA**

* Protocol and Electrical Compliance Testing of SATA, USB, and Thunderbolt devices.
* Setup LeCroy, Keysight/Agilent and other gigahertz scopes for electrical testing.
* Setup SATA protocol tester.Setup LeCroy,
* Tested thunderbolt devices on Apple Macintosh computers spanning range of thunderbolt chip sets.

**7/2014-10/2014, Traveling in South Korea and then Japan as a tourist.**

* I have an AA in Japanese so like to visit Japan to practice Japanese.

**9/2013-4/2014, Took an Android course and wrote some android programs including space invaders**

**1/2012-8/2013, Studied Verilog/VHDL in FPGAs using Xilinx ISE(now Vivado) and Altera Quartus II**

* Modified VHDL Apple II to work on a Altera FPGA board I have.
* Made functional model of an Apple II including VGA, PS/2, and game port drivers. Used a 6502 CPU from opencores.org.
* Currently 1/2016 making gate level Apple II in Xilinx Vivado Tools.

**9/2011-11/2011, Temporary Software Engineer, Western Digital, San Jose, CA**

* Wrote C++ code to process a capture file from a IOTracer Utility.
* Setup Clonezilla on a USB Flash Drive to configure or restore Fedora Linux and hard drive partitions on Dell Servers.
* Setup a variety of VMWare virtual Windows and Linux systems.

**8/2007-6/2010, Manufacturing Test Engineer, Ericsson, San Jose, CA (formerly Redback Networks)**

* Created diagnostic functional test scripts for Ericsson's IP Ethernet Broadband line cards using ProComm Aspect.
* Supported SE100 test fixture maintaining TCL test scripts running under Linux.
* Tested on-board data links between PPA2 chips, DIM FPGA, Back plane and front network ports. Ran data with boards in feedback modes and also used external feedback cables and passed data between line cards out front ports and through the back plane. Continually updated, tested and identified issues with new board FPGA and VxWorks images and brought issues to respective teams.
* Used lab tools to identify problems such as failed DC-DC converter, damaged components, bad memory, BGA connection problems.
* Supported and visited contract manufacturers such as Plexus in Fremont and Jabil Circuits in San Jose and Guadalajara Mexico to train technicians with tests on new line cards and to help with board debug.
* Maintained and updated test fixtures online at remote contract manufacturers.
* Developed technical documents for engineering review meetings.
* Updated agile database with line card test scripts and FPGA and VXWorks images.

**2/2005-12/2006, ASIC Validation, Tharas Systems Inc., Santa Clara, CA**

* ASIC Validation. Wrote validation code in C, TCL, and custom microcode for the fourth-generation of a hardware EDA accelerator.
* Loaded up the system by setting memories and configuring many muxes. System consisted of one or more boards with each board having 8 copies of our custom ASIC.
* Ran payloads through the data paths, and checked results. Found and documented numerous errors involving manufacturing flaws, timing problems, reset problems, and Xilinx FPGA rocket I/O link problems.
* Developed many tests for manufacturing and lab use, as well as some diagnostics for running test clusters. Went through the ASIC's Verilog and talked to the system architect to see how to test the system.
* Wrote microcode for the custom CPU for running many millions of cycles and calculated or wrote C code to calculate expected results. My work contributed to the eventual successful bring-up of the system.
* Tharas Systems wasn't getting enough POs so had to merge with Eveteam.com.

**7/2004, C Programmer, NASA Ames Research Center, Mountain View, CA**

* Brief Engineering task. On Winkler Project - a precision gamma ray detector that was being refurbished at NASA Ames. Read old 8085a firmware with my EETools EEPROM programmer.
* Found an 8085 disassembler written in old style C with original type of function parameter declarations. Modified it to run under Linux and disassembled the original 8085 image.

**11/2001-3/2003, Firmware Engineer, Rasvia Systems, Sunnyvale, CA**

* Wrote embedded C code running under VxWorks for a 9 disk fibre channel storage array.
* Performed many embedded software tasks as part of the development of the RAID storage array. Wrote firmware for the cache-board that ran on the MIPs core of an enclosure management chip (Vitesse VSC120). Configured various ports and pins, including FC-AL, I2C/SMBus, GPIO, interrupt and serial ports,
* Used I2C chips and the VSC7147 to run hardware fibre channel device bypass tests.
* Upgraded the I2C driver on the controller boards when I encountered an infinite retry bug.
* Wrote code to validate the fibre-channel loop (by issuing LIP's) and communicated the state from the cache board to the controller.
* Programmed the FPGA. Optimized the code for speed. Wrote a wrapper to compress the code so that two FPGA image copies could be stored.
* Found hardware bugs involving the board configuration and connections.

**4/2000-11/2001, Firmware Engineer, Sun Microsystems Network Storage, Newark, CA**

* Software debug for Sun's T3 mid-range storage array which was modified from a similar Maxstrat storage array. Made a version of the build system which used gcc since it identified many errors which the PSOS compiler missed.
* Used openboot F-code, a version of Forth, firmware on a low-end storage array being developed. The array used a Sun motherboard and a custom board with a PCI bridge and PCI to IDE chips along with IDE drives. Wrote diagnostics to probe the I2C and PCI buses.
* Discovered existing bugs in Openboot involving the I2C and PCI Bridge drivers. Used cscope and scripts to trace through the Openboot source code to find bugs.

**7/1998-8/1999, Firmware Engineer, Cyclonics Inc., Fremont, CA**

* Designed algorithm and wrote all the Verilog for the remote control's audio search pattern identification chip and tested it in an Altera FPGA. Used Synopsys dc\_shell and Galileo to compile the Verilog.
* Logic-design and debug in verilog and DVD player firmware in C.
* Modified the player's firmware which was running in an ICE. Changes enabled the state of the machine to be monitored by using its remote control and on screen display(OSD).
* The MPEG chip had several error counting registers which were important to monitor. found many errors such as problems passing data between two clocks and problems at some DVD format block numbers. When there were problems playing audio CD's studied source verilog and found that head and tail pointers of the input buffer could pass each other and even flip left and right audio channels.

**6/1997-9/1997, Summer Internship, NTT MCL, Palo Alto, CA**

* Wrote a CGI program which would call some network monitoring tools. Made a web page where tools and times could be selected to monitor network traffic. Data from the tools were written to files and graphed by gnuplot onto web pages.
* Played enough lunch time soccer games to be awarded the rare, coveted and highly prestigious NTT MCL Jalapenos T-Shirt.

**4/1996-9/1996, C Programmer, Lockheed Martin, Palo Alto, CA**

* Wrote some passes of a C-like compiler.

**6/1995-9/1995, Firmware Engineer, Sun Microsystems, Newark, CA**

**6/1989, Summer Academy English Tutor, Osaka YMCA, Tosabori-dori Osaka, Japan**

**PROGRAMMING LANGUAGES AND DEVICES:**

* C under VxWorks on disk array.
* Java on Android Device and under Linux.
* C firmware on DVD player running inside ICE. Debugged FPGAs and used on screen display.
* Controlled I2C/SMBus devices and debugged driver which had infinite retry bug.
* Controlled PCI bus manually under openboot/openfirmware BIOS.
* FPGA logic design. Designed and implemented audio pattern detector for remote control.
* In C Monitored Fibre Channel Loop. Checked device addresses.
* Debugged address/data bus with logic analyzer.
* Assembly(6502,8086,68HC11,68000,RISC), C/C++, Verilog, FPGA, Java, Android, TCL, Bash
* gcc, Turbo-C++, Visual C++, eclipse, netbeans, octave(mathematica).

**HDL LANGUAGES:** Verilog, Xilinx ISE, VHDL, Altera Quartus, Maxplus II, Synopsys dc-shell.

**RECENT EXPERIENCE:**

**6/2016-current,** Learning Xilinx Vivado FPGA tools with Artix-7 FPGA board and Android. Using SDK to incorporate Microblaze soft core processor into Verilog design.

**5-12/2015**- TCL/Expect

**10/2014-** Android

**7-10/2014,** More than three months trekking around South Korea and Japan.

**5/2014,** Machine learning course from Stanford University using Octave(Matlab compatible).

**12/2013,** Android course from Foothill College.

**8/2012,** VLSI Certificate after five courses: SystemVerilog and FPGA design.

**EDUCATION:**

9/2010-9/2012 – UC Santa Cruz Extension: VLSI Certificate.

6/2010-6/2011 – Foothill College: AS Biology.

9/1996-6/1998 – UC Santa Cruz: MS Computer Engineering.

9/1993-6/1995 – UC Santa Cruz: BS Computer Engineering with highest honors.

3/1987-6/1991 – Foothill College: AA Japanese.