Fabrication and testing of a MEMS-based optical filter combined with a HgCdTe detector

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ABSTRACT

The Mid-wave infrared (MWIR) spectrum has applications to many fields, from night vision to chemical and biological sensors. Existing broadband detector technology based on HgCdTe allows for high sensitivity and wide range, but lacks the spectral decomposition necessary for many applications. Combining this detector technology with a tunable optical filter has been sought after, but few commercial realizations have been developed. MEMS-based optical filters have been identified as promising for their small size, light-weight, scalability and robustness of operation. In particular, Fabry-Perot interferometers with dielectric Bragg stacks used as reflective surfaces have been investigated. The integration of a detector and a filter in a device that would be compact, light-weight, inexpensive to produce and scaled for the entire range of applications could provide spectrally resolved detection in the MWIR for multiple instruments. We present a fabrication method for the optical components of such a filter. The emphasis was placed on wafer-scale fabrication with IC-compatible methods. Single, double and triple Bragg stacks composed of germanium and silicon oxide quarter-wavelength layers were designed for MWIR devices centered around 4 microns and have been fabricated on Silicon-On-Insulator (SOI) wafers, with and without anti-reflective half-wavelength silicon nitride layers. Optical testing in the MWIR and comparison of these measurements to theory and simulations are presented. The effect of film stress induced by deposition of these dielectric layers on the mechanical performance of the device is investigated. An optimal SOI substrate for the mechanical performance is determined. The fabrication flow for the optical MEMS component is also determined. Part of this work investigates device geometry and fabrication methods for scalable integration with HgCdTe detector and IC circuitry.

Keywords: MWIR, Fabry-Perot interferometer, MOEMS, Bragg reflector

1. INTRODUCTION

1.1 Motivation

The spectral range from 3-5 μm has recently been of great interest due to its variety of applications in chemical sensing and astronomy, as numerous gases have very distinct absorbance bands in the region. Detectors in this region can have very high sensitivity, but due to their wide-band response, the spectral resolution is very low. Large mechanically controlled optical filters that have been added to the system, although of high resolution, are costly and are hard to adapt to all the desired applications. It is our goal to create technology that would combine the highest quality detector and filter components to create devices that have high sensitivity and spectral resolution, are low-cost, easy to manufacture and can be implemented in a wide variety of applications.

1.2 Previous work

Large Fabry-Perot interferometers have been made for astronomy purposes since 1970s[1]. Lately there has been work on creating small, light and inexpensive filter/detector devices, starting with NIR and moving into MWIR and LWIR [2]. Scaling down infrared detectors allows them to be coupled with MEMS-based optical filters in several ways. Integration in a package has been done by the InfraTec Corporation, which has created a commercial product based on a Fabry-Perot filter made out of several layers of bonded silicon wafers, with Bragg stack mirrors made out of silicon and silicon dioxide layers[3]. Schuler et al. gives an excellent summary of theory and extensive overview of several technologies[4]. Monolithic integration has been done by the University of Western Australia group, who have been working on

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monolithic integration of a HgCdTe detector with a MEMS filter, that uses a Bragg stack composed of germanium and silicon oxide layers on a silicon nitride structural layer[5].

1.3 Short review of Fabry-Perot interferometer principles

A typical Frabry-Perot device is illustrated in Fig. 1. Light with intensity Ii is incident on a thin film of thickness t. Some of the light is reflected, Ir, and some of the light is transmitted, It. The two mirrors have reflectivity R and are separated by a gap of distance d. Constructive and destructive interference of light incident on the face produces a filtering effect, allowing light of wavelength md/2 (m is an integer) to pass through, reflecting all others[6].

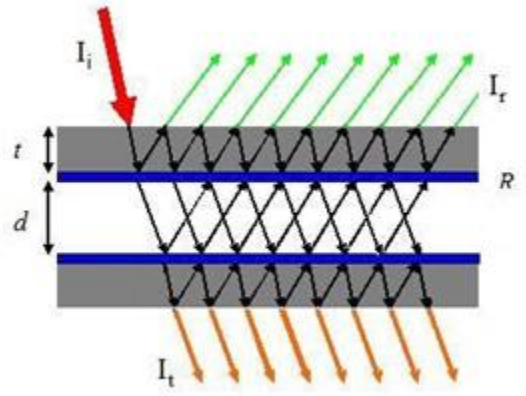

Figure 1. Illustration of a Fabry-Perot interferometer.

The main figure of merit of a Fabry-Perot interferometer is reflective finesse, given by[6]

—

——— (1)

The full width at half maximum (FWHM), or bandwidth, is

——— (2)

For the majority of applications, it is of particular interest to increase the finesse of the filter and decrease the bandwidth, as this would allow for higher spectral resolution.

1.4 Overview of the device

The overall goal of this project is the fabrication of the Fabry-Perot filter integrated with HgCdTe detector and CMOS circuitry, as shown in the Fig. 2. The device that was fabricated as filter is a MEMS interferometer based on mechanical parts consisting of one movable membrane, supported by springs at the corners (X-beam) and one stationary membrane[7]. The structural material is silicon, and the reflection in the MWIR region is enhanced by deposition of Bragg stacks on the surfaces of the two mirrors. The Bragg stacks consist of alternating layers of silicon oxide and germanium, chosen for their linear index of refraction in the MWIR. Germanium was chosen for the highest index of refraction of materials easily processed in the standard IC fabrication environment, and silicon oxide was chosen for the smallest index of refraction. A stack composed of these layers gives high reflectivity and therefore high finesse in a Fabry-Perot interferometer. The thicknesses of the layers are chosen equal to a quarter-wavelength at 4 μm. The back of the movable membrane could be covered with an anti-reflection coating (ARC) consisting of silicon nitride with a half-wavelength thickness.

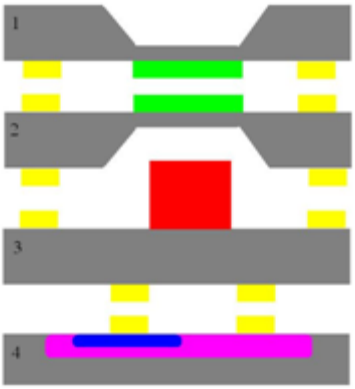

Figure 2. Proposed integration mechanism to create a complete device out of filter layers (1 and 2), HgCdTe detector layer (3) and CMOS control and logic layer (4).

2. PROCESS DEVELOPMENT

2.1 Mechanical layer

The geometry of the Fabry-Perot interferometer lends itself easily to use as a standard MEMS parallel-plate actuator, where two opposite plates separated by a small distance are moved together when the opposite charge is accumulated on the two surfaces. The electrostatic actuation of this device requires the two surfaces to be electrically conductive and mechanically stiff. The optical design requires these layers to have low absorption in the MWIR. The material that answers all of these requirements is silicon, with low absorbance and well-characterized mechanical properties. To decrease the absorbance, it is desired to use as thin a layer as possible, with the lowest doping that would still produce the desired electrostatic actuation.

Commercially available silicon-on-insulator (SOI) wafers provide high-quality and low-cost thin silicon layers without the need to develop this process. While single-crystalline silicon has no intrinsic stress, SOI wafers, due to processing, have intrinsic stress in the device layer that is sometimes very high. The thickness of the device layer, thickness of the buried oxide layer (BOX), and the method of bonding have influences on the stress in the released structures.

Two different configurations of SOI wafers purchased from Ultrasil Corp. have been evaluated: 10 μm device layer with 2 μm BOX, and 25 μm device layer with 0.3 μm BOX.

As the intrinsic stress in the device layer can have a detrimental effect on the final device, there is a need to measure it in each configuration. Bow-tie structures, shown in Fig. 3, have been used to measure the stress in-plane wich has been measured to be 200 MPa compressive in the 10 μm device layer, and 5-10 MPa compressive in the 25 μm device layer.

In order to define the X-beam and provide isolation trenches on the chips, the silicon device layer has to be etched. The handle wafer has to have windows etched through it to provide a clear optical path for light.

Two etching processes have been developed to etch the device layer: HF/nitric/ncetic acids (HNA) wet etching and a deep reactive ion etch (DRIE) process based on sulfur hexafluoride (SF6) plasma. The HNA etch has the benefit of being low-cost and allows etching of many wafers at the same time, but it is not selective to other materials used in the process and the etch rate varies greatly with time and temperature. The DRIE etch produces very repeatable etch rates and is very selective to all other materials, so it does not require extra depositions of protective materials, but it is limited in through-put[8].

The handle wafer was etched by two processes, the wet TMAH etch and the dry DRIE process. The benefits and drawbacks are the same as for the wet and dry etch processes for defining the device silicon.

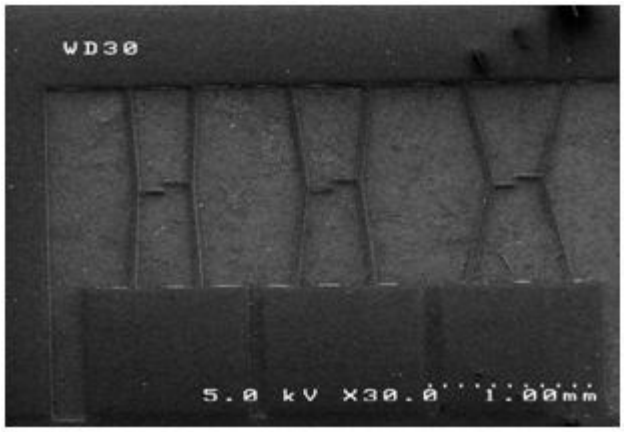

Figure 3. Fabricated bow-tie test structure.

2.2 Mask layout

The design of the mask has chips for both the fixed membrane and the movable membrane supported by the X-beam actuator arms on the same wafer, to prevent wafer-to-wafer variability. The layout is presented in Fig. 4, and shows a 4" wafer layout. Bow-tie stress test structures are located on the perimeter of the wafer.

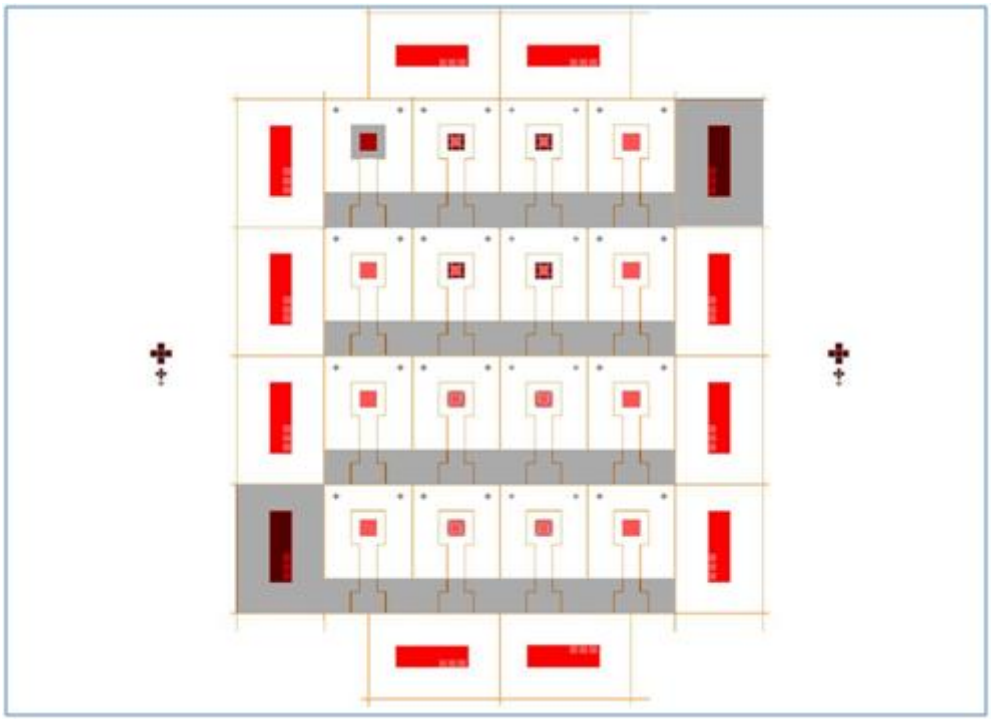

Figure 4. Wafer layout.

2.3 Mirror materials and optical results

Fabry-Perot mirrors have to have high reflectivity (99.9% in commercially available devices) and low absorption[4]. Metal mirrors would have high reflectivity, but the absorption is very high in the MWIR and LWIR ranges. Bragg stacks composed of dielectrics with quarter-wave thickness are traditionally used. The mirror is composed of alternating layers of materials with high and low indices of refraction, and an approximation of the reflectivity is given in Eq. 3,

where n_0 is the index of refraction of the incident media, n_1 and n_2 are indices of refraction of the two materials that make up the stack, and n_s is the index of refraction of the substrate[9].

(3)

The reflectivity is increased with a higher number of high-low refraction pairs and an increase in the difference in the index of refraction of the two materials. In order to decrease complexity and therefore cost of the fabrication process, it is desirable to keep the thickness of the mirrors and the number of pairs to a minimum. The layers used have to be commonly available and not require special processing, since not many commercial foundries have capabilities to handle some of the more exotic materials that have desirable indices of refraction.

After considering some of the standard MEMS processes and materials and their optical properties in the MWIR range, it was decided that germanium and silicon oxide would be utilized. Both of those materials have almost perfectly constant index of refraction in the desired range and are widely available.

While high-quality films of monocrystalline and polycrystalline germanium with well-studied optical properties can be grown using CVD furnaces, it is also possible to deposit germanium using an e-beam evaporator at the same cost as metallization layers in CMOS. While the crystalline structure is of lower quality than CVD films, the quality becomes comparable when depositing multiple pairs on an underlying amorphous silicon oxide. Using films deposited on silicon wafers, it was determined that a germanium film of 250 nm thickness had a stress of 90 MPa tensile.

Silicon oxide films for the mirrors were deposited using a PECVD process at 350^o C. While the resulting layers are of lower quality than films deposited using CVD, the lower temperature of deposition allows lower stress in the resulting layers, and decreases the oxidation of the germanium layers. After initial testing, it was determined that films deposited using a low-frequency plasma had much higher stress than layers deposited using a high-frequency plasma. The lowest stress achievable in silicon oxide films deposited in this system was 190 MPa compressive.

The deposited layers were evaluated using SEM imaging to ensure the proper thickness and quality of the films. Figure 5 shows a cross-section of a test wafer with a double Bragg stack, consisting of two silicon oxide layers 720 nm thick and two germanium layers 250 nm thick. In the image, one can see a defect in the silicon oxide layer caused by particle contamination on the surface of the preceding germanium layer. Extra cleaning steps between depositions have eliminated this defect for the following depositions.

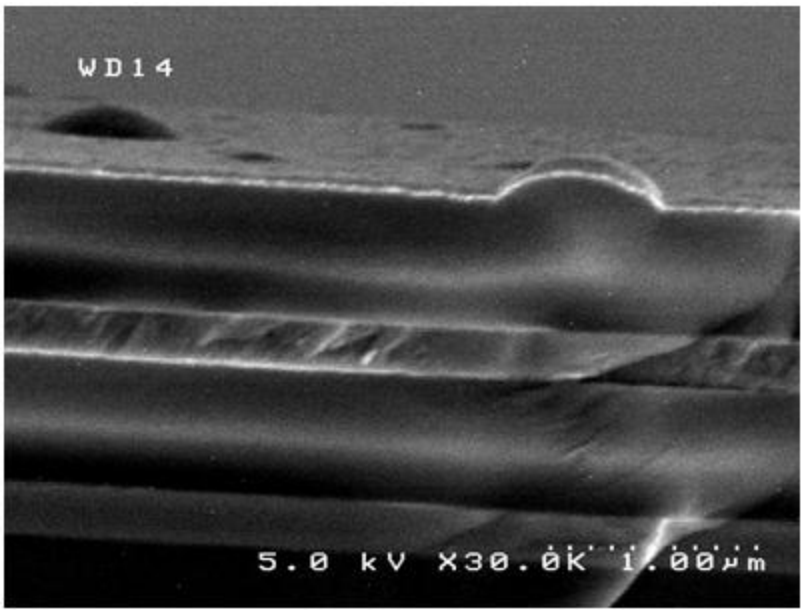

Figure 5. SEM image of double Bragg stack.

For the purposes of optical testing, a range of test wafers was fabricated, with single, double and triple Bragg stacks deposited on silicon wafers.

Two etching processes were tested for etching of the Bragg stacks. Both processes used a hard mask consisting of 20 nm of chromium and 100 nm of gold. The first process used a combination of two etchants, 6:1 buffered oxide etch (BOE) for silicon oxide and hot (70 degrees) phosphoric acid for germanium. It was determined that the two etchants are perfectly selective to the other layers. Consequent etching of silicon oxide and germanium layers for a triple Bragg stack produced undercuts of 5 microns, which is small compared to the dimensions of the structure. A second etching process used a single etchant, HNA, to etch both materials in one step. Both processes produced undercuts of more than 5 μm, as can be seen in Fig. 6.

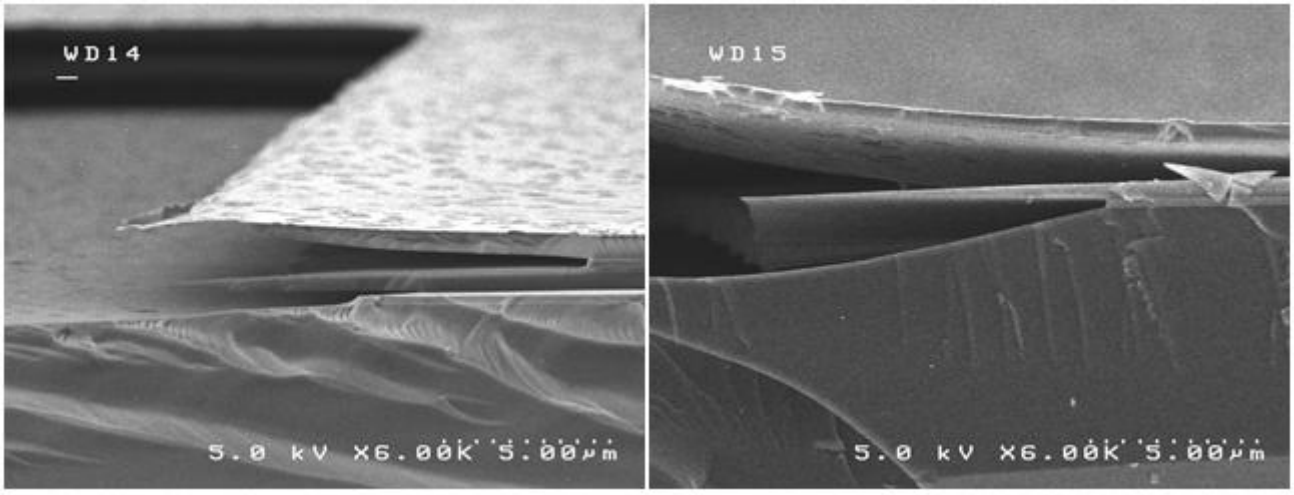

Figure 6. SEM Undercuts in triple Bragg stack produced by HNA etching (left) and consecutive etching (right).

An anti-reflective coating (ARC) consisting of 500 nm layer of silicon nitride was developed as part of the process. The index of refraction of silicon nitride corresponds to the requirements of wide-range ARC[10, 11].
Silicon nitride was deposited using PECVD system, which allows for a mix of high and low-frequency plasma deposition. A range of film stress from 290 MPa compressive to 550 MPa tensile for a film of 500 nm thickness can be controlled by selecting the right frequency mix.
Optical testing has been performed on these wafers, in order to confirm simulations of the Bragg stack reflectivity. Fig. 7 plots the result of these tests, normalized to the reflectivity of a wafer coated with gold. As can be seen from this figure, a triple pair of germanium-silicon oxide layers produces a reflectivity close to 98% in the 3-6 μm range.

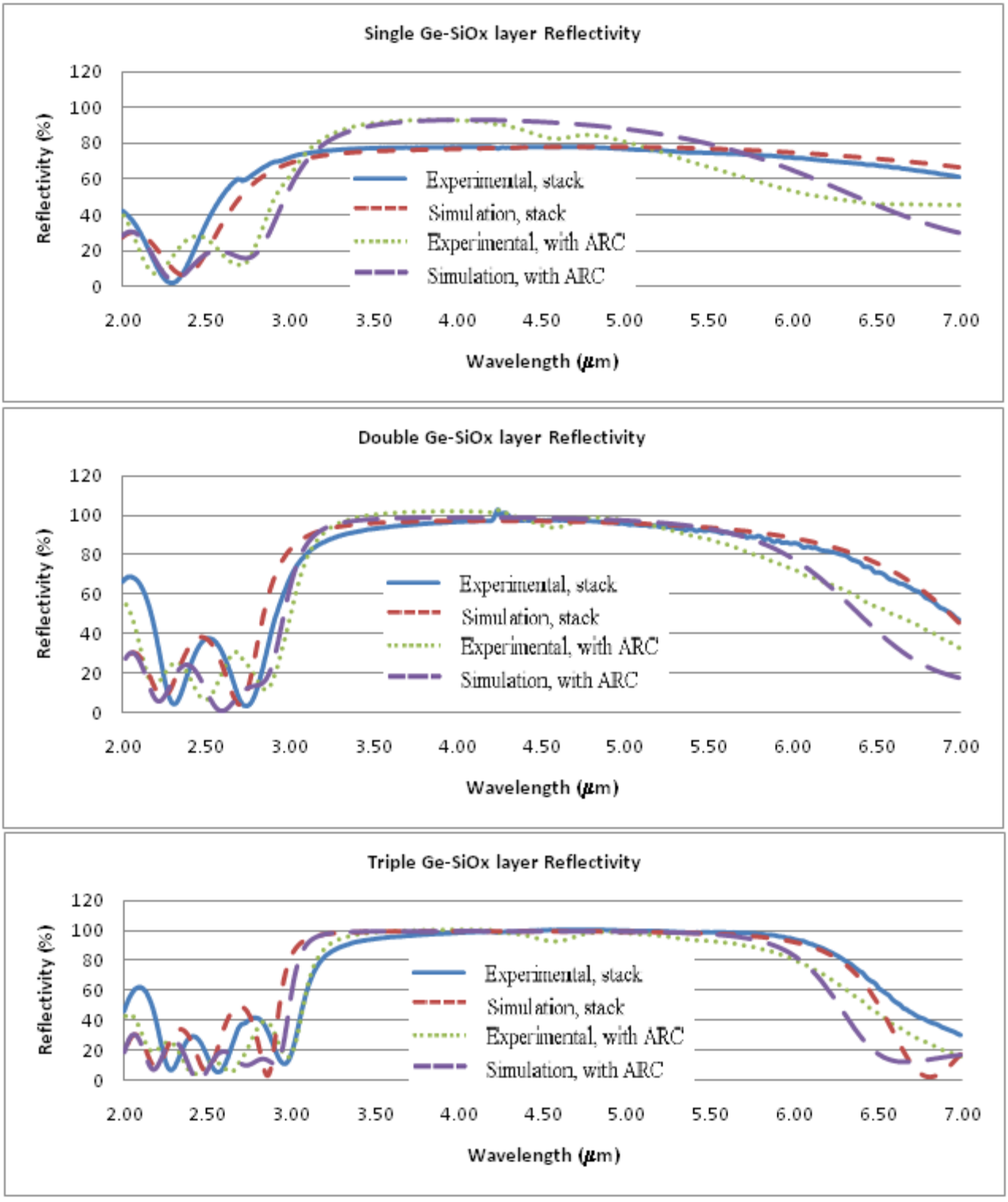

Figure 7. Reflectivity of single, double and triple Bragg stacks, normalized to the reflectance of a gold wafer.

While the triple Bragg stack has the required reflectivity for the optical behavior of the filter, the layers would produce a film with a total of 300 MPa compressive stress. A triple Bragg stack was deposited on top of a silicon wafer, and a 1mm square window was etched from the substrate, creating a suspended membrane. Buckling of the membrane, as seen in Fig. 8, shows that high levels of stress would produce a structure that is far from the desired, perfectly level mirror.

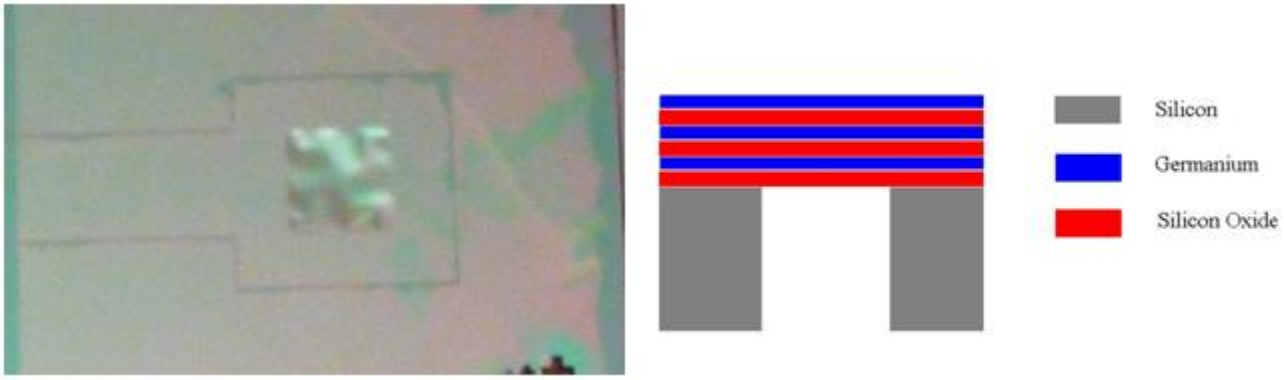

Figure 8. SEM image of double Bragg stack.

Table 1. Stress levels in relevant layers used in fabrication.

Material	Method of deposition	Thickness	Stress
Silicon Oxide	PECVD	720 nm	190 MPa compressive
Germanium	E-beam evaporation	250 nm	90 MPa tensile
Silicon Nitride	PECVD	500 nm	600 MPa compressive – 450 MPa tensile
Membrane silicon	SOI wafer	10μm, 25 μm	200 MPa compressive, 5-10 MPa compressive

2.4 Surface Roughness

The surface roughness in the mirror produces widening of the transmitted peak[12]. The desire for high spectral resolution requires reducing the roughness as much as possible, given the surface roughness of the starting wafer. As there are several processes that could be used for each step, a process matrix was evaluated according to the combination of the steps used and the resulting roughness of the mirrors.

It was determined that the highest roughness, on the order of 400-500 nm, resulted from HNA etching of the Braggs stack, HNA etching of the device layer, and TMAH etching of the handle wafer. Apart from high roughness of the surface, there were numerous pinholes through all the layers.

The best surface, with a roughness of 19.2 nm, was produced with consequent etching of the Bragg stack and DRIE etching of the device silicon and handle silicon, as can be seen in Fig. 9. The defects were minimized, and the surface roughness is just slightly higher than the surface roughness of the starting wafer.

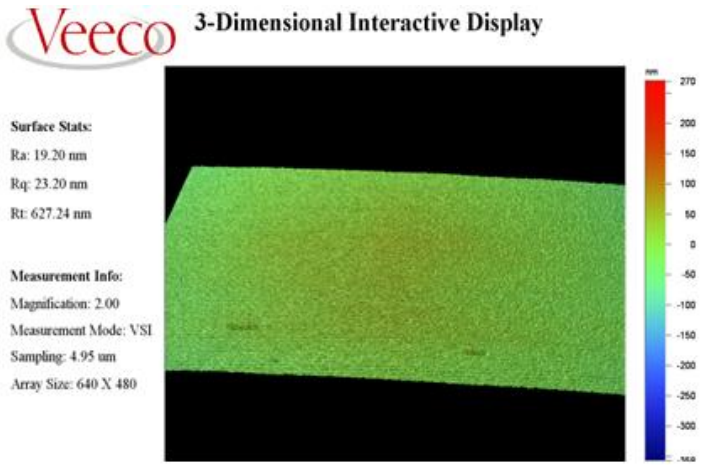

Figure 9. Bragg mirror surface produced with the best step combination.

2.5 Stress-induced bow

High levels of stress in the deposited materials produce deformation in the released membrane and X-beam components. Table 2 summarizes the deformations obtained using two different SOI wafers. A combination of thicker silicon device layer with lower stress produces the lowest deformation, while the thinner silicon device layer with a higher stress produces the largest deformation. Additionally, the defects such as pinholes localize the deformations, producing extremely asymmetrical shapes. Fig. 10 shows surface scan of an X-beam fabricated on 25 μm silicon device layer with a low defect density. The deformation has been exaggerated for improved visualization.

Table 2. Stress-induced bow in fabricated components.

SOI wafer and part	Bow
10 μm device Si, membrane	2.17 μm
10 μm device Si, X-beam	15.3 μm
25 μm device Si, membrane	67 nm
25 μm device Si, X-beam	3.7 μm

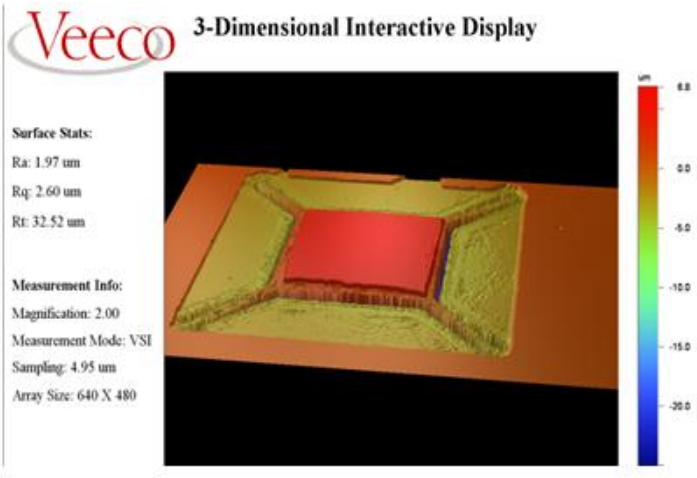

Figure 10. X-beam part produced on 25 μm silicon device layer with triple Bragg stack.

In order to further decrease the bow, thicker silicon device layers have to be used in conjunction with stress compensating layers.

3. CONCLUSION

In this work, we have completed the first round of fabrication and optical testing of the chips used for a Fabry-Perot interferometer filter that will be combined with HgCdTe detector. Analysis of several steps of the process was performed in order to combine the steps that produce the devices with lowest surface roughness and the least stress deformation. The resulting process is high-yield, uses only materials that are widely available and compatible with HgCdTe detector integration. Further work is required to reduce the bow of the X-beam structures.

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