Wafer-scale fabrication of a vertically-aligned NEMS switch based on carbon nanofibers

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ABSTRACT
Fabrication of nanoscaled transistors based on carbon nanotubes and inorganic nanowires is typically demonstrated with a "pick-and-place" or similar method which allows for fabrication of small numbers of transistors at a time. While these, and other, devices have been used to demonstrate potential applications of carbon nanotubes, these methods are not applicable to wafer scale production with large yield. Carbon nanofibers (CNFs) show great promise as potential mechanical elements in nanoelectromechanical system (NEMS) devices while their vertical orientation allows for integration into standard vias or other devices with an inherently low footprint. Here, we discuss a CMOS compatible wafer-scale fabrication scheme for scalable production of carbon nanofiber based NEMS switch devices. Well dimensions are defined by standard photolithography approaches and e-beam lithography is utilized for CNF catalyst definition. A multi-stack trench etch is used to define wells in which CNFs are grown using the commonly employed PECVD method. Integration issues related to multi-layer etch and CNF growth conditions are also presented. This approach demonstrates promise for integration of a low-footprint, high-performance NEMS device into a CMOS process flow.

INTRODUCTION

Keeping up with computer scaling will require novel types of devices. MEMS devices are very promising for their speed, on/off ratios, and Q factors. Reducing the size of such devices requires utilizing novel materials. The carbon nanofiber (CNF) appears to be a good alternative to micromachined cantilever beams due to its low Young's modulus, straightness and growth from a catalyst.[1] One such use of CNF is as an electromechanical switch or relay. Some uses of such a device would be in memory applications, programmable logic, and chemical/biological sensors. CNFs grown by PECVD inherently possess a vertical orientation. This allows for their integration into a vertical well architecture, which decreases the size of

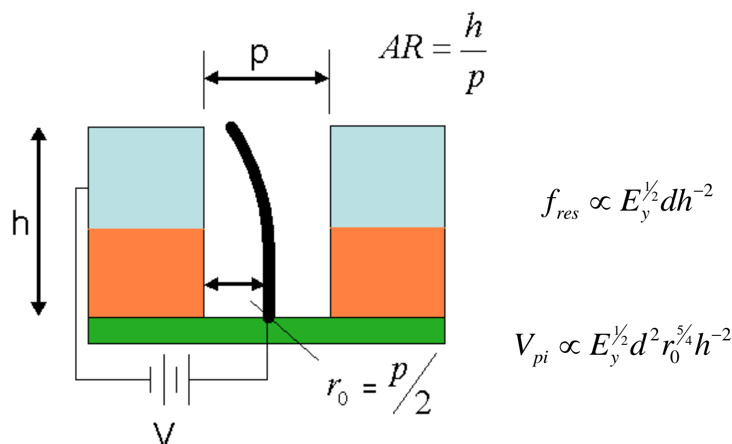


Fig. 1 Vertical well device with catalyst-grown CNF as switching element

device and allow for multiple states of operation, compared to a horizontally oriented device.

In previous work, we showed that this device, depicted schematically in Fig. 1, yields a pull-in voltage that increases as the 5/4 power of gap spacing, and decreases with the square of height.[2] Thus, to provide a low pull-in voltage to fit within the requirements of low-power electronics, the well requires a high aspect ratio. For operation under 10 V, the aspect ratio would have to be at least 3:1 [2].

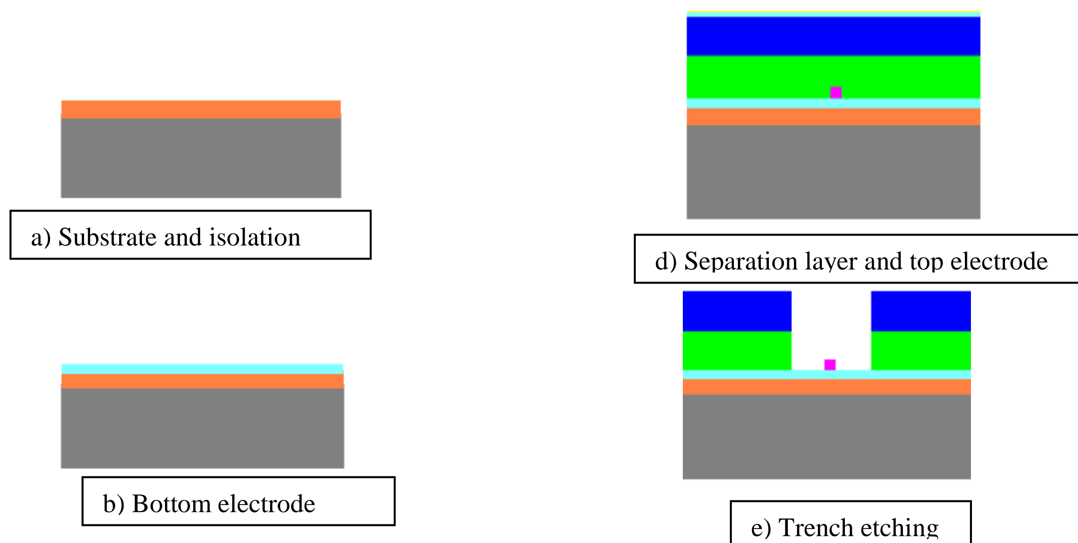
Such a device would have to be fabricated on wafer scale to compete with CMOS and traditional MEMS processes. Two technologies that have rapidly advanced in recent years make it possible: PECVD and nanolithography.

PECVD chambers have been used in the industry for decades for depositions of dielectrics, but use of PECVD for growth of CNF is a relatively recent development. From initial experiments using bare two-inch chambers, advancements have been made to the use of four-inch chambers with built-in heaters. It is only recently that commercial systems have been available with six and eight inch electrodes, with precise control of heat and growth parameters. Use of such systems would allow large-scale production of CNF-based devices.

Patterning of a catalyst on nanoscale requires a lithography systems that can provide accuracy and uniformity across the wafer. The Raith 150 e-beam system allows for wafer-scale patterning of nanometer features. Although the throughput of e-beam lithography is still too slow for a manufacturing process, it allows demonstration of device fabrication. Meanwhile, higher throughput lithography systems with nano-scale resolution, such as extreme UV [3] or nanoimprint lithography [4], are becoming increasingly close to meeting the needs of industrial large-scale fabrication. For high-throughput manufacturing, these techniques can be used in place of e-beam lithography without changing the process flow to a significant extent.

EXPERIMENT (process)

The fabrication of the vertical well structure is a bottom-up process, therefore the major steps were layer deposition and subsequent patterning to create the structure desired. The process flow is summarized in the figure below:



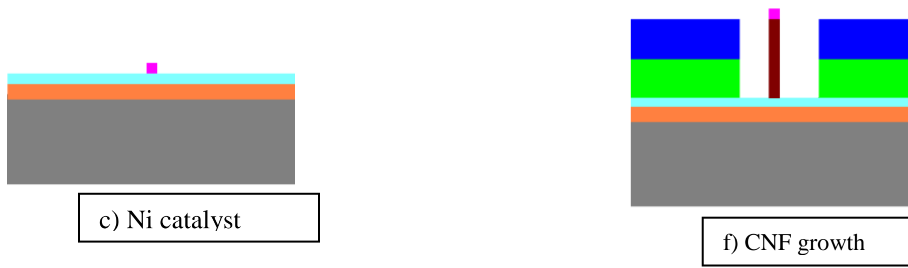


Fig. 2 Cross-sections through a CNF device after each major step n the process flow

The process includes deposition of an isolation layer over the substrate, followed by a patterned bottom electrode. The catalyst is deposited on the bottom electrode. The whole wafer is then covered by a dielectric separation layer, with the top electrode as final structural layer. The trench is etched over the catalyst through all the layers, as well as contact pads to the lower electrode. The CNF is grown using PECVD.

The process required three photolithography masks, one for the bottom electrode, one for the trench region etch, and one for patterning of the top electrode. These masks were optimized for inter-layer capacitance and resistance.

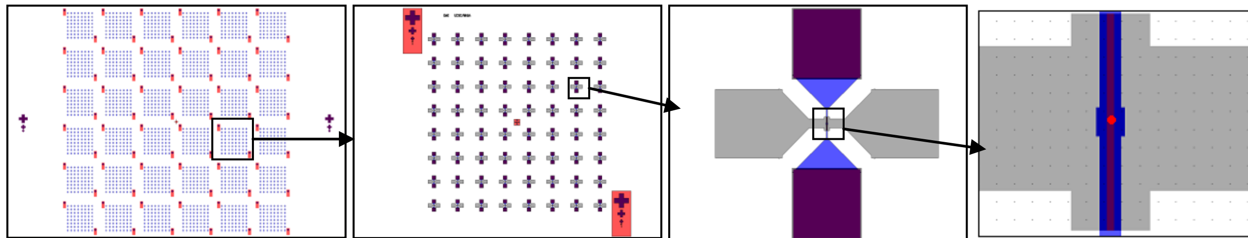


Fig. 3 Three photolithography mask combination from wafer lever to trench

Each chip on the wafer is designed to provide a range of trench sizes from 1 to 8 μm and have CNF diameters from 20 to 70 nm. In this way, on a single wafer, 64 devices of different parameters are created, allowing us to investigate properties of the switch.

The substrate is a standard four-inch Si wafer. In order to isolate the substate from the devices, a 300 nm thick isolation layer of PECVD-deposited silicon nitride is used. Material choices for the bottom electrode and catalyst are driven by our earlier combinatorial studies in metal combinations suitable for CNF growth.[5] Initially, 30 nm of titanium was used due to its higher electrical conductivity. However, it was later changed to Cr for process compatibility (see below). Measurement of the electrode conductivity indicated negligible difference between Ti and Cr electrodes. The lower electrode is patterned with optical lithography, followed by metal lift-off. After the bottom electrode is patterned, the catalyst deposition is performed, making use of alignment marks in that layer. E-beam lithography for this step uses 100 nm 2% PMMA resist. The thickness of this resist was a determining factor for the thickness of the bottom electrode, as the uniformity of this resist from the spin-coating process is dependent upon the topography of the lower electrode. Following exposure and development in a Raith 150 e-beam

lithography tool, a Ni film is deposited, and lift-off defines the final catalyst dimensions. The lift-off process is a far easier method of defining catalyst dots than trying to etch them from a blanket film. Next, to separate the top and bottom electrodes and increase the height of the well, a dielectric layer is deposited. For this layer, we used a 0.5 μm thick PECVD silicon dioxide. The top electrode layer used is 0.5 μm thick tungsten, deposited by e-beam evaporation. Oxide-tungsten delaminating problems were solved by depositing a thin titanium adhesion layer in the same tool. Finally, a 10 nm thick chromium hard mask layer is deposited.

To avoid lithography alignment challenges, it was decided to etch the entire trench in one sequence rather than to define trenches independently in the different layers. This required a three step etch process to deal with the different materials and selectivity requirements. First, the selectivity of the tungsten etch relative to photoresist was sufficiently low that a chromium hard mask was required. The hard mask was patterned using photolithography and a CR-14 wet etch for 15 s. Due to the thinness of the Cr layer, the isotropic wet etch was acceptable for defining the trench opening. The underlying W layer is completely resistant to CR-14 etch. Using the resulting hard mask, the top (W) electrode and Ti adhesion layer are etched in a SF_6 plasma for 7.5 minutes. During this etch, no hard etch stop is required and partial etching of the underlying dielectric is acceptable. The Cr hard mask was then removed by wet etch in Cr-14 for 30 s, allowing the electrode layer to now serve as the hard mask. The SiO_2 separation layer is then etched using $CHClF_2/O_2$ anisotropic plasma etch for 20 min. For reasons to be discussed below, this step does not result in complete removal of SiO_2 from the trench region and instead is timed to leave an oxide layer on the bottom electrode that is 10s of nm thick. Finally, a wet HF etch is performed to remove the last SiO_2 in the trench region and expose chromium bottom electrode.

RESULTS AND DISCUSSION

Patterning the catalyst particle required a series of tests of the e-beam lithography system. These tests included different photoresist thicknesses and test pattern fabrication. Such test patterns include range of dosages to determine dosage-size correspondence, as well as optimizing the development time for the range of dimensions desired. A range of dosage was found that produced the desired dot sizes, with transfer of that process from test chips to wafer-scale test pattern writing, and finally to writing catalyst dots on the device wafer. Initial trials were performed using the dots from the test pattern to determine parameters for PECVD CNF growth to produce optimal fibers, as seen in Fig. 4

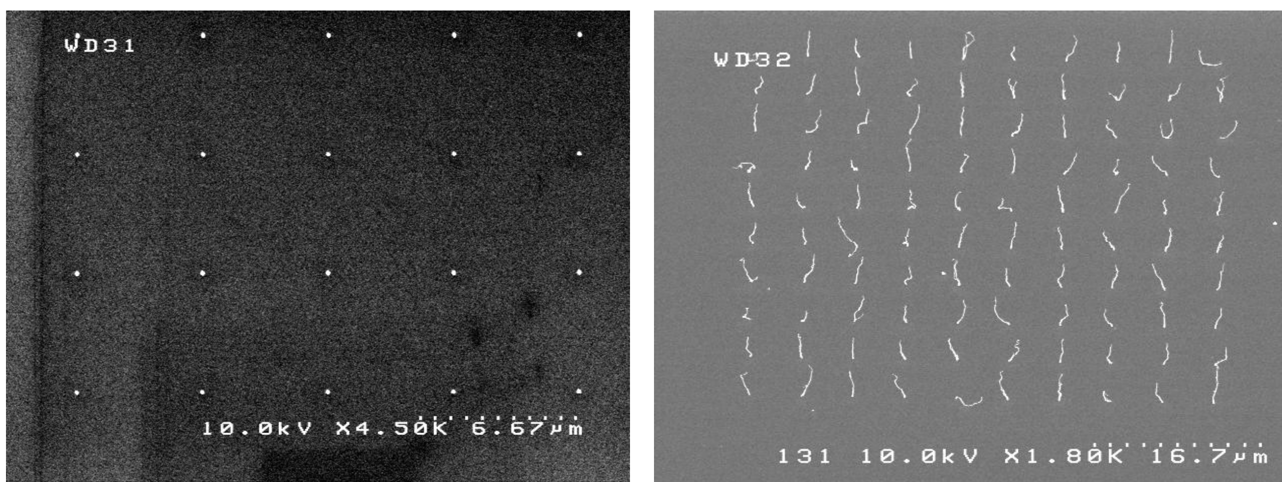


Fig. 4 Catalyst dots in test pattern, with pitch of 5 μm in order to minimize proximity effects between individual fibers, and initial CNFs grown from them (growth parameters not optimized)

The majority of problems encountered were during the multi-step etch process. Significant topography was observed in the trench region following the oxide etch as shown in Fig 5. This topography is often observed as “micromasking” in plasma etching, where an etch-resistant material is deposited into the trench and masks portions of the film, causing them to etch more slowly. Through a series of experiments, we determined that this micromasking was most likely caused by sputtering of the Cr hard mask during the metal etch step, causing a pattern to be transferred into the oxide etch. This was resolved by reducing the plasma etch power during the W etch, and also stripping the Cr layer off prior to the oxide etch. Reducing the plasma power in this step also resolved a second problem, which was underetch of the W film, also shown in Fig 5. The underetch indicated an isotropic component to the metal etch, which was likely exacerbated by heating of the substrate by the relatively high plasma power.

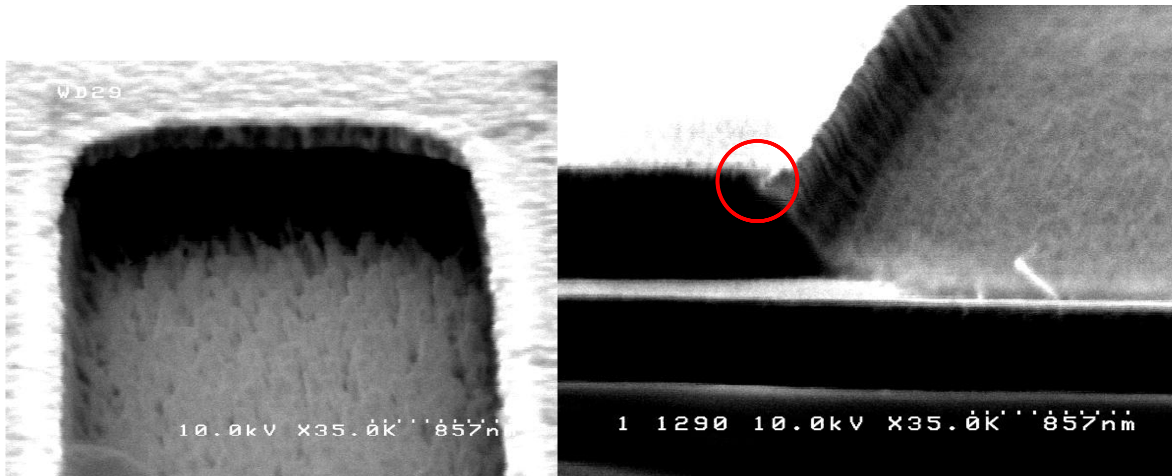


Fig. 5 Trench etching with oxide pillars on the bottom electrode resulting from micromasking by sputtered Cr film, and undercut in top tungsten electrode as result of aggressive etch

After solving the micromasking problem, it was still found that a rough residue remained on the surface after the dry SiO_2 etch. This residue came in the form of several small granules, as shown in Fig 6, which obscured the presence of any catalyst on the bottom electrode, and no CNFs could be grown from this surface. Electrical tests on the lower electrode indicated very high contact resistances resulting from the residue. Auger spectroscopy revealed the composition to be a mixed $SiO_xC_yF_z$ layer. This type of byproduct is not uncommon from an oxide etch. Attempts to remove the residue by conventional methods were largely unsuccesful. More aggressive approaches to removal resulted in destruction of the bottom electrode. It was finally determined that stopping the etch process prior to completion and leaving approximately 20 nm of oxide on the surface would allow an HF dip to remove the underlying oxide layer and take the residue off with it. This process required switching the bottom electrode material from titanium to chromium in order to avoid damage to the electrode by the HF.

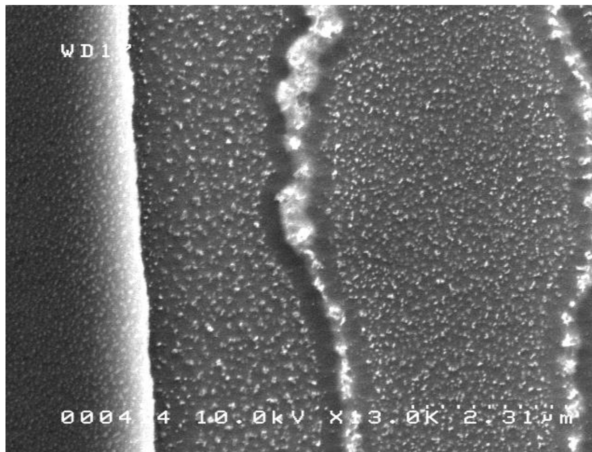


Fig. 6 Residue on the bottom electrode

Devices that were fabricated after resolving the above-mentioned challenges are presented in Fig. 7 below. The structure visible in the first part is the top electrode (light color) with contact pads for the bottom electrode; in subsequent pictures, the trench region is shown, with the lower electrode in the bottom of the trench formed by the separation layer and the top electrode. The surface of the bottom electrode is free of etching residue. Under high magnification (100K), a catalyst particle can be seen in the middle of the bottom electrode.

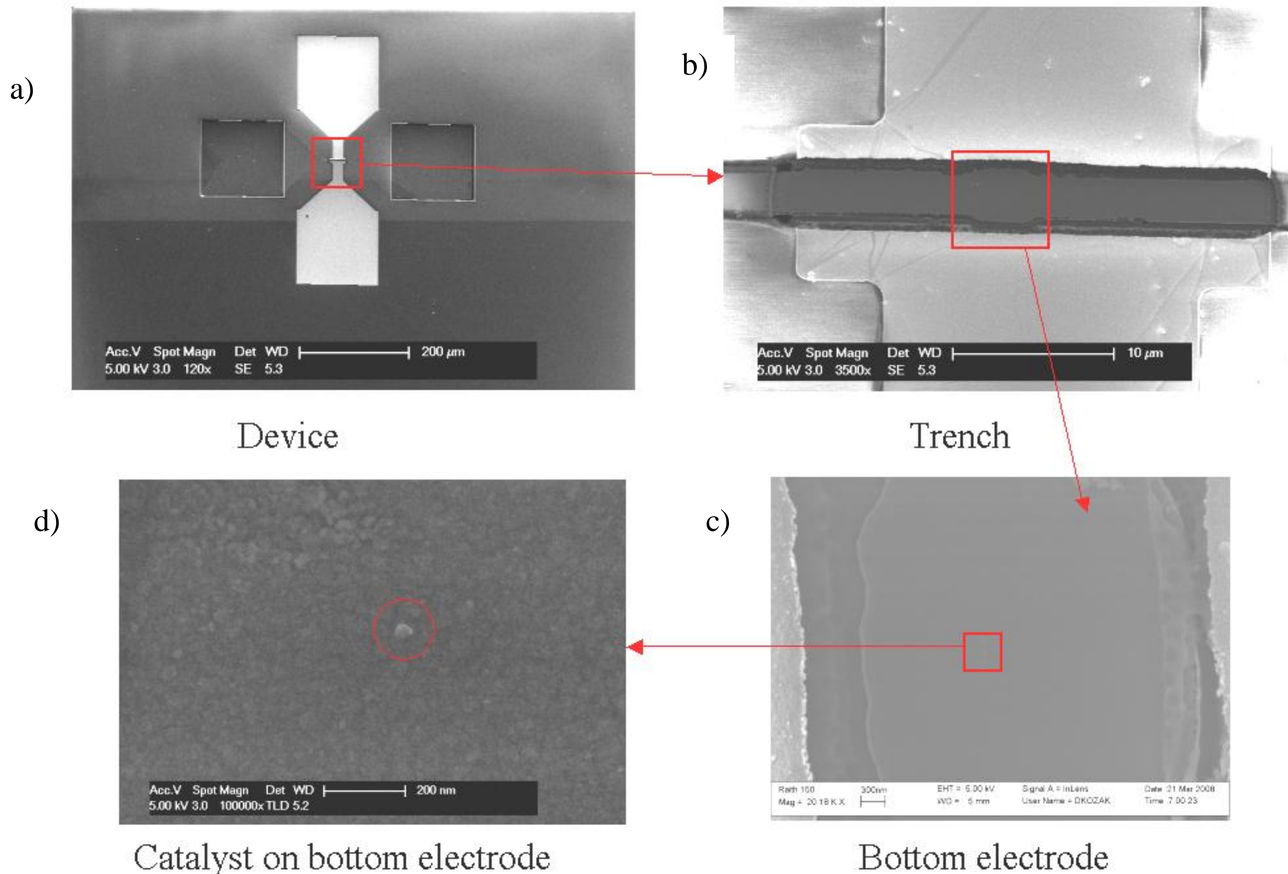


Fig. 7 SEM images of the fabricated device: a) Entire device, with contact pads for the bottom and top electrode, magnification 120x; b) Trench region, with bottom electrode in the bottom of the trench, magnification 3500x; c) Bottom electrode, magnification 20Kx; d) Catalyst particle on the bottom electrode, magnification 100Kx

Finally, integration with the PECVD growth of the CNF introduced additional challenges, as evidenced by the SEMs in Fig. 8. First, charge buildup on the oxide surfaces in the PECVD chamber resulted in microarcing between the top and bottom electrodes, which destroyed the trench region. Second, the high temperatures of the PECVD process (> 600 C) resulted in formation of bubbles on the surface, most likely resulting from hydrogen gas trapped within the PECVD oxide layer.[6] The solutions to these problems are ongoing. The first problem results from the DC plasma process that results in a net positive charge flux to the lower electrode. Anecdotally, this has been solved in other systems by reverse pulsing the dc discharge or by introducing a third porous electrode directly above the wafer at the same potential [7]. This electrode serves to shunt part of the plasma current away from the device wafer and attempts to perform PECVD with this in place are currently underway. We have determined that the second problem is absent at temperatures of 600 ºC or below, which is consistent with literature reports.[8] Thus, either lower temperature deposition processes are required, or a pre-deposition anneal step may drive off trapped gases without causing blistering. These experiments are currently underway.

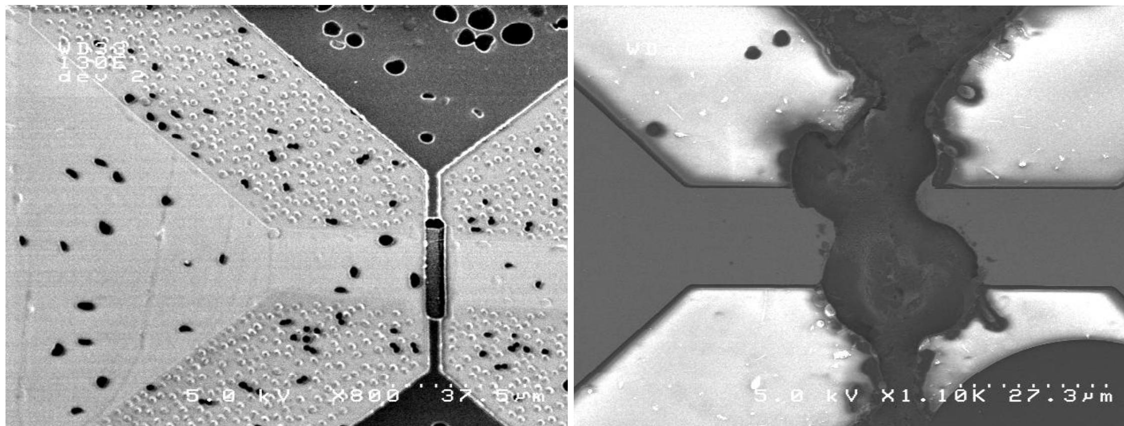


Fig. 8 Thermal damage and microarcing after PECVD

CONCLUSIONS

A process for fabrication of a CNF-based switch has been developed. We have developed the proper layer combination and relative thicknesses for the prototype device, as well as means of patterning them to achieve the desired structure with the least complicated processes possible. Optimization of the masks and etching parameters has been performed whenever possible. This process is simple and robust, allowing for variations in layer thicknesses without significant changes to the process. It was proven that such a device could be made on wafer scale, using standard IC fabrication tools. Several challenges unique to the architecture of the device have been resolved. Integration with PECVD process of CNF growth is yet to be perfected. Parameter space is to be found that results in the best CNF properties (length, mechanical properties, shape) that would result in minimal damage to the structure.

FUTURE WORK

The future work on this project in the short-term is primarily the PECVD growth of CNF on fabricated structure. This would entail solving the above-mentioned problems, as well as finding the optimal growth conditions (i.e. pressure, temperature, gas ratio). Once the initial proof-of-principle devices are fabricated, the next step would be to develop the process further to improve the characteristics of the device.

In the development of the process, the simplest and most robust photolithography techniques were used. To improve the performance of the device and optimize the architecture, we would prefer to use more advanced photolithography. Availability of new tool, ISML I-line system, would allow us to pattern trenches on the dimensions of 300 nm, thus greatly reducing the operating voltage. Use of smaller trenches would require development of more precise etching techniques.

Characterization of resulting devices would allow us to better understand the behavior of the switch. An analytical model should be developed to include the effect of architecture on the performance of the switch, including such parameters as height and trench width. Once such a model is developed, architecture of the device could be modified to be application-specific. For applications that would require low pull-in voltage (such as memory or logic) new devices would have to be fabricated, using thicker separation and metal layers and narrower trenches. Fabrication of these specific devices would involve further development of the process.

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