Poly-Phase Fractional-N Frequency Synthesizer

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Abstract

The aim of this thesis is to present a phase-hopping frequency synthesizer using a Rotary Traveling Wave Oscillator (RTWO), as well as the benefits and limitations of physical realizations. The RTWO is a novel approach to Integrated Circuit (IC) Voltage Controlled Oscillator (VCO) design that employs a differential transmission line terminated on itself in a manner similar to a Möbius strip. Because the RTWO is a geometric construct, it enjoys an availability of precise phases, limited only by transmission line length and minimum feature size in the metal interconnect layers. The system described in this paper consists of a 1GHz, 62-phase RTW-VCO and a poly-phase divider technique[3] that offers 62 division channels per octave up to the oscillator frequency. To increase the spectral coverage, a fractional-N technique is used in the feedback path of the Phase-Locked Loop.

1 Introduction

With the increase in popularity of wireless communications, consumer demands on wireless systems have also increased. A modern wireless network is required to support many users, provide higher data-rates, work at a longer range, and follow governmental regulations, all at a reasonable cost. The common, and cheapest, solution is to employ digital modulation schemes such as Phase Shift Keying (PSK) and Quadrature Amplitude Modulation (QAM) to increase the effective bit rate/Hz, and different multiplexing methods (e.g. Time-Division Multiplexing (TDM), Frequency-Division Multiplexing (FDM)) to allow more users per frequency channel. As a result there are numerous standards across the radio spectrum, each serving a different purpose and user group.

The motivation behind this work is a US Congressional decision to establish a new level of inter-operability among government entities[1]. This ruling requires Public Safety Agencies (PSAs) (Police, Fire, Medical, Navy, National Guard, Air Force, FAA, ...) to communicate with each other over several wireless standards. In other words, PSAs need a universal radio system that can tap into their networks. The frequencies allocated to these agencies range from 30MHz up to 1GHz[2], and each network employs some form of trunking[1], frequency-hopping[2], or other modulation scheme. In order to satisfy the inter-operability requirements, a new radio system needs to cover a very broad frequency spectrum and meet each individual network's specification. Presently, the most economical way to meet all these needs this is to include several different radio modules into one physical package and switch between the modules depending on the network. The frequency synthesizer presented here is intended to serve as an affordable broad-band carrier source for future generations of public safety radios, making it possible to use one software configurable radio module to access a wide range of wireless network standards. As such, the spectral purity,

[1] Trunking is a combination of TDM and FDM, building on the fact that voice communications cannot fully utilize the bandwidth of a channel. As such, a trunking system assigns users transmission windows for a data packet

[2] Popular in military communication systems due to an immunity to narrow-band interference, requires very agile carrier sources[4].

frequency tuning, phase noise, and agility requirements for the synthesizer are quite stringent.

2 Background

A major constraint of many frequency synthesizer systems is the division ratio between the VCO and the output frequency. In dynamically programmable systems, the divisor between VCO and output frequency is limited to integral values ($f_{out} = f_{vco} \div N;\ N \in \mathbb{N}$), and in the case of high speed VCOs, it can be limited to only even integers or powers of 2 ($N = 2^M;\ M \in \mathbb{N}$)[3]. This severely reduces the spectral coverage provided by a synthesizer, resulting in dead bands or coverage gaps. To reduce this limitation, a typical solution is to increase f_{vco}, which creates more division channels and increases power consumption, sensitivity to parasitics, and the complexity of the division circuitry. One alternative to increasing f_{vco} is to employ the novel poly-phase division technique as described later in this thesis, the other alternative is to use a fractional-N technique.

2.1 Phase Locked Loops

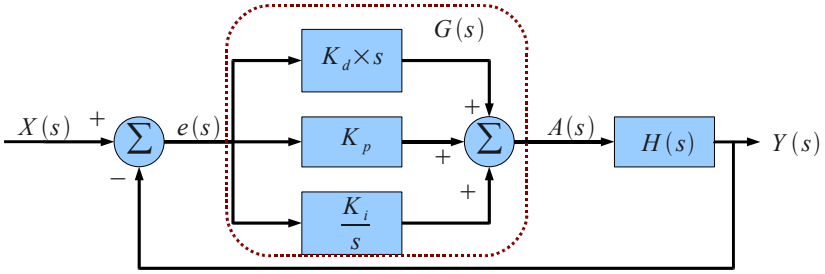


Figure 1: Proportional Integral Derivative (PID) controller.

A PLL is a type of a negative feedback control system that adjusts a VCO such that its output frequency is at a ratio of a reference oscillator frequency.

[3]A patented new divider technology (The Spot Divider) has demonstrated odd, even, and some half (e.g. 4.5) division ratios at upwards of 6GHz in a 0.18um CMOS process, while maintaining low power and low phase noise.

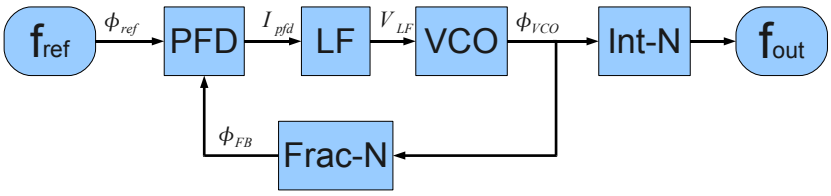


Figure 2: System level block diagram of a PLL system.

Typically, these systems are modeled in s-space, through the use of Fourier and Laplace transforms of the governing equations[4]. Fig. 1 is a classical example of a control system. The three terms (*proportional*: K_p; *integral*: $\frac{K_i}{s}$; *derivative*: $K_d \times s$) constitute the controller *G(s),* which provides a control signal *A(s)* to a physical system *H(s)* such that its output *Y(s)* follows the control system input *X(s)*. The *proportional (P)* component determines the immediate system response to an error. The *integral (I)* term (*pole*) accumulates any error and zeroes out *e(s)* effectively equaling infinite gain at DC. It should be noted that an integration results in a delayed action. Unless damping is introduced through a *derivative (D)* term (*zero*), a system is likely to overreact and possibly become unstable. However, a derivative term can end up amplifying high frequency input, an effect that is undesired in most tracking systems. Careful *pole* and *zero* placement is essential for system stability and responsiveness.

Fig. 2 represents a system level diagram of the synthesizer. The reference sources comes in as a phase ramp ϕ_{ref} with slope f_{ref}. The Phase Frequency Detector takes the difference between ϕ_{ref}, ϕ_{FB} and based on that, injects a small charge $I_{CP}{}^{(\phi_{ref}-\phi_{FB})/2\pi}$ into the Loop Filter, where I_{CP} is the current through the charge pump[8]. The 2^{nd}-order loop filter in this system consists a large capacitor that integrates the input current into a control voltage V_{LF} and a pole-zero pair for system stability $\left(\frac{s+1/\tau_1}{s(s+1/\tau_2}\right)$, where τ_1 and τ_2 are the time constants of the filter. The VCO can be represented as a black-box $\left(\frac{K_{VCO}}{s}\right)$

[4]The response of a system is the convolution of the input signal with its impulse response. Attempting that operation in the time-domain involves solving the Green function for the system and a lengthy convolution integral. Finding the impulse response in s-space is a matter of evaluating a Laplace or a Fourier transform, and the convolution integral is reduced to an algebraic multiplication.

that integrates a tuning voltage into an output phase ramp ϕ_{VCO}. The last component of the feedback system is the feedback divider, which scales ϕ_{VCO} by some ratio $\frac{1}{N}$. Combining all these pieces produces the following sets of equations and the closed loop gain of the synthesizer (Eq. 1)[5].

$$I_{pfd} = I_{CP} \times (\phi_{ref} - \phi_{FB})$$

$$V_{LF} = I_{pfd} \times \left(\frac{s+a}{s(s+b} \right)$$

$$\phi_{VCO} = V_{LF} \times \frac{K_{VCO}}{s}$$

$$\phi_{FB} = \phi_{VCO} \times \frac{1}{N}$$

$$\frac{\phi_{VCO}}{\phi_{ref}} = \frac{\frac{K_{VCO}}{s} \frac{s+a}{s(s+b)} I_{CP}}{1 + \frac{1}{N} \frac{K_{VCO}}{s} \frac{s+a}{s(s+b)} I_{CP}} \tag{1}$$

2.2 Fractional-N Synthesizers

The idea behind a fractional-N synthesizer is quite simple: switch between two or more different frequency channels at a given rate, such that the average frequency passed to the output is the one desired (Eq. 2, where τ_n is the time spent in channel n until switching to a different channel). Since the switching is controlled by a deterministic state machine, it will produce a repeating pattern with a period of $\tau_{pattern} = \sum_n \tau_n$. For a fixed pattern, most of the energy from the switching action will appear at $f_{spur} = \frac{1}{\tau_{pattern}}$ and several other discrete frequencies, depending on the pattern. There is no way to eliminate this switching energy, but techniques do exist that can spread it in the output

[5]For a more detailed explanation of this kind of a PLL refer to W. Keese[8].

spectrum, so that it does not overwhelm any single frequency band (Fig. 3).

$$f_{out} = \frac{\sum_n f_n \tau_n}{\sum_n \tau_n} \quad (2)$$

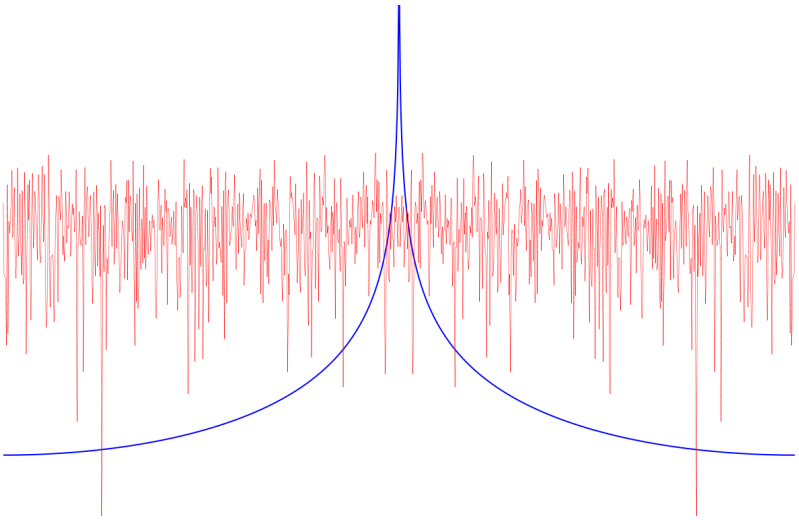
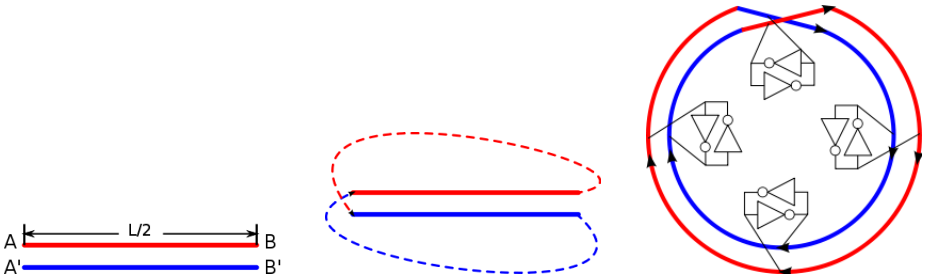


Figure 3: FFT logarithmic plot of periodic switching between two frequencies (thick blue line) and random switching (thin red line). The time spent in each of the two channels is approximately the same, so the average output frequency is the same in both examples. The integrals of the power spectra are also the same $\int F_{periodic} df \approx \int F_{random} df$. The power in the periodic switching is concentrated at the switching frequency, while the power in the random switching is spread out across the spectrum. If the periodic switching is kept at a frequency higher than the 0dB point of Eq. 1, the spur power will be attenuated and that approach may be practical. Alternatively, the random switching will spread the switching power into the higher frequencies, where it will be attenuated by the loop filter, and into the lower frequencies, where it will raise the noise floor of the system. If an increased low frequency noise floor is intolerable, the best solution may be find ways to push out the spur from periodic switching into the higher frequencies.

Without special care, this fractional channel approach generates plenty of undesired spectral content in the output, that can severely degrade the performance of any system utilizing a fractional-N synthesizer. Conventionally this problem has been addressed by including the fractional-N divider in the feedback path of a PLL system (see Fig. 2), such that the unwanted frequency



(a) (b) (c)

Figure 4: a) Differential transmission line, b) terminated on itself. c) RTWO with regenerative amplifiers distributed along the transmission line.

content is filtered by the loop filter.

2.3 Rotary Traveling Wave Oscillators

An RTWO is a differential transmission line terminated on itself, forming a conducting loop with the following spatial boundary conditions Eqs. 3 & 4. Distributed along the transmission line are back-to-back inverters that suppress the symmetric even modes, allow only differential modes along the transmission lines, and provide power to overcome resistive losses.

$$V(x,t) = V(x+L,t) \tag{3}$$

$$V(x,t) = -V(x+{}^{L}/_{2},t) \tag{4}$$

Eq. 3 establishes that only periodic or constant spatial solutions can exist, and Eq. 4 eliminates all even mode solutions, where x is the position along the total length L of the conductor. Given that an RTWO is an electromagnetic structure, it obeys Maxwell's equations, from which we can derive Eq. 5. Solving the wave equation for the system with all the spatial boundary conditions results in a traveling wave solution of the form in Eq. 6, where $f_0 = {}^{1}/\sqrt{LC}$. [6] [5]

$$\frac{\partial^2 V}{\partial x^2} = \frac{1}{\gamma^2}\frac{\partial^2 V}{\partial t^2} \tag{5}$$

[6] L and C are the inductance and capacitance, respectively, of the transmission line.

$$V(x,t) = DC + \sum_n A_n sin\left(2\pi n\left(f_0 t - \frac{x}{L}\right)\right),\ \{n = odd\ \mathbb{N}\} \tag{6}$$

Eq. 6 supports traveling waves in both the $+x$ and -x directions. For a symmetric ring with sufficiently high gain, spontaneous symmetry breaking occurs due to noise that exists in the dominance of only one direction of wave propagation. In practical applications, the direction of the traveling wave must be known and set in the design process. That is done by making travel in one direction more energetically favorable than the other direction, by introducing some asymmetry to the resonant structure[5]. Since for most RTWO implementations, the physical location from which the wave is observed is fixed, Eq. 6 reduces to $V(t) = DC + \sum_n A_n sin(2\pi n f_0 t),\ \{n = odd\ \mathbb{N}\}$[7].

3 Synthesizer System

3.1 Basic Principles of Operation

The phase-hopping integer-N division technique uses the spatial term in Eq. 6 in a way very similar to the frequency shift due to the Doppler effect (Fig. 5). Eq. 6 is transformed into Eq. 7, by changing the physical location of the readout position at a given rate relative to f_0 (62 is the number of phases in this RTWO, *Inc* is the number of taps hopped, *(62+Inc)* is the number of taps in the modified period).

$$x = vt \Rightarrow \left(\frac{Inc}{62 + Inc}\right) L f_0 \times t$$

$$V(t) = DC + \sum_n A_n sin\left(2\pi n f_0\left(\frac{62}{62 + Inc}\right) t\right),\ \{n = odd\ \mathbb{N}\} \tag{7}$$

To reduce the timing constraints on a physical implementation, the next active tap is selected in the direction of the traveling wave, such that the output frequency is always equal to or lower than the frequency of the RTWO.

The one drawback of phase-hopping division is that variations in the various

[7]For a more in-depth study of rotary traveling wave oscillators, refer to G. Mercey[5].

propagation delays between phase taps and output can give rise to periodic phase modulation and hence undesired spurs. Any circuitry that is along the tap-to-output path can add a delay depending on where the circuit is laid out on the silicon wafer. Additionally, naturally varying process parameters, such as MOSFET threshold voltages, can add a significant amount of mismatch between propagation paths, resulting in Eq. 8.

$$V(t) = DC + \sum_{n} A_n sin\left(2\pi n f_0 \left(\frac{62}{62 + Inc}\right) t + \phi_{mismatch}(t)\right), \ \{n = odd\ \mathbb{N}\} \tag{8}$$

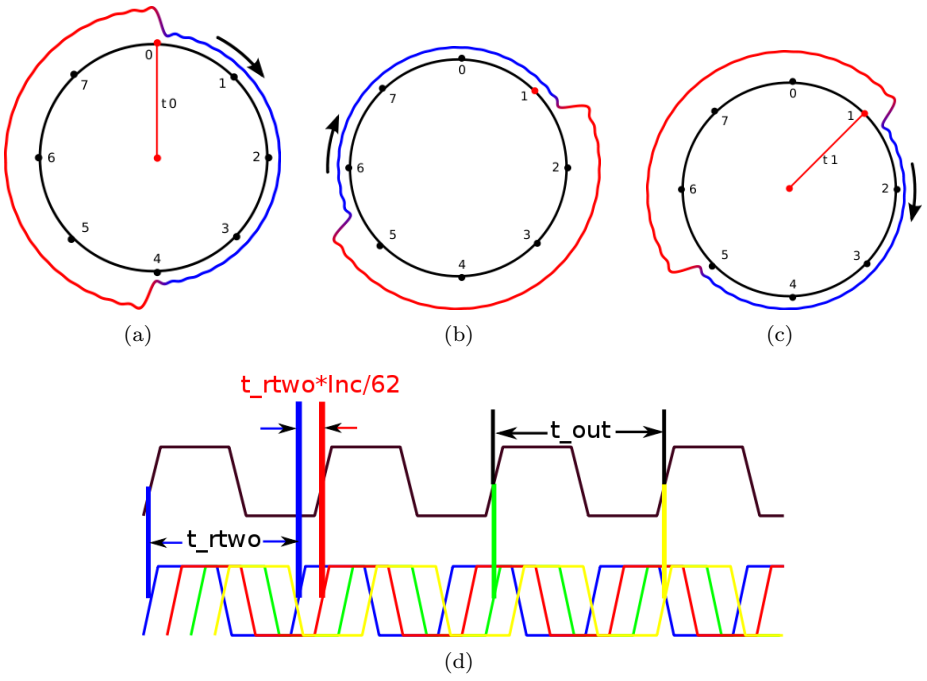


Figure 5: Phase Hopping Technique, incrementing by 1. a) Tap 0 is active and reads the rising edge of the traveling wave. b) With the falling edge, tap 0 is deactivated and tap 1 is prepared for the next rising edge. c) Tap 1 is active to read the rising edge. In this sequence, the period of the output of the RTWO (schematically taken at the center of the ring) is scaled by $\frac{8+1}{8}$. d) Timing diagram of phase-hopping division.

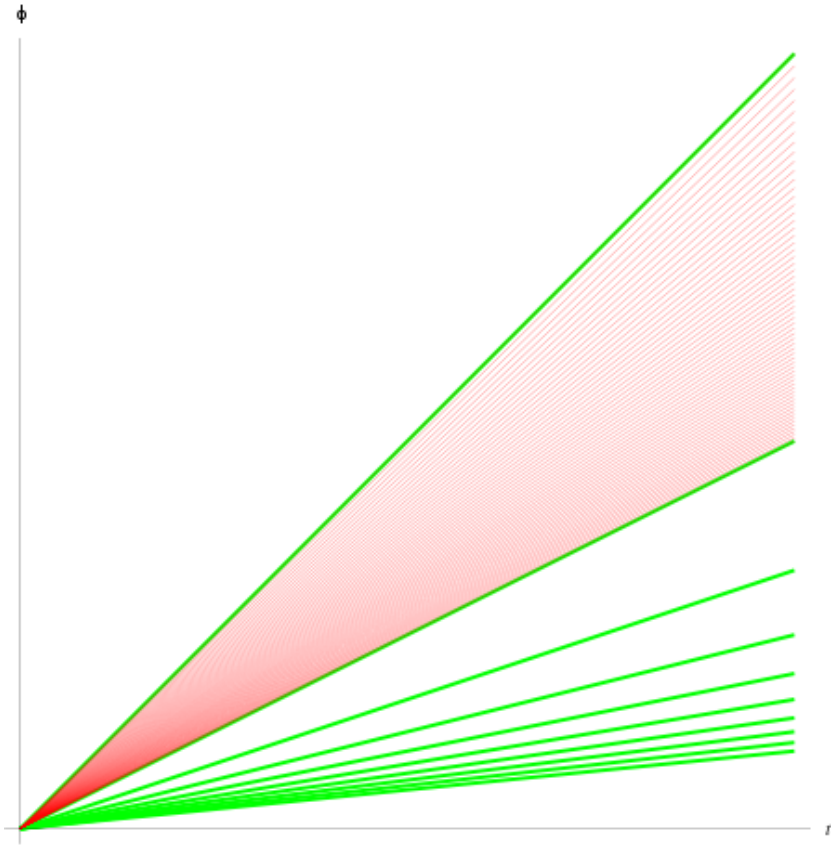


Figure 6: Phase ramps of poly-phase divider (thin red lines) covering one octave, and integer-N divider (thick green lines) for divide by *1 through 10*. The slope represents output frequency.

3.2 System Overview

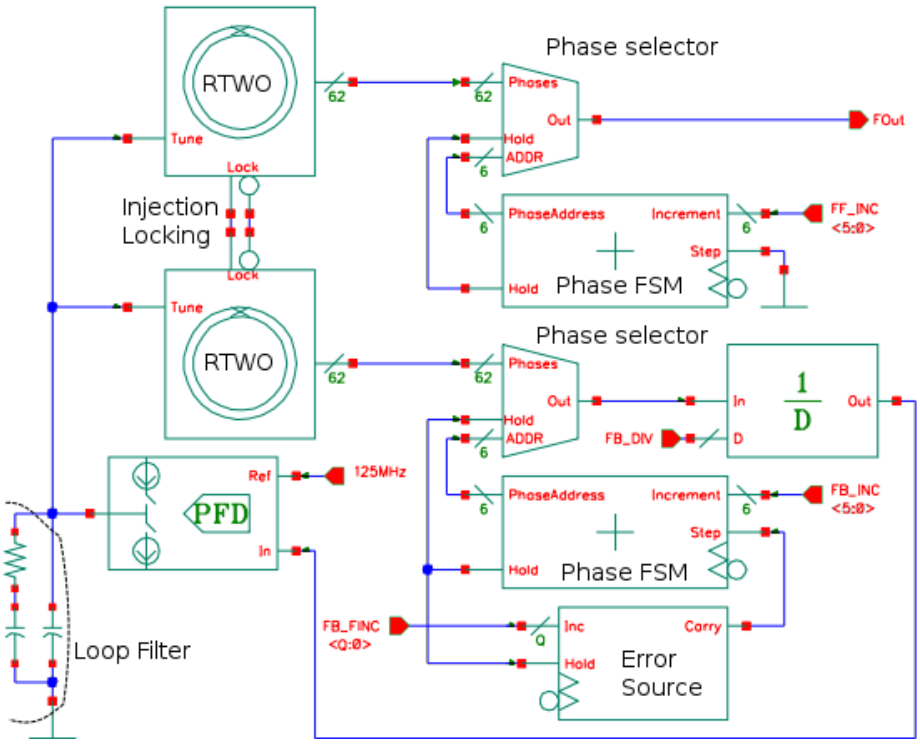


Figure 7: Fractional-N Synthesizer System.

The synthesizer system is designed with two identical injection locked and inductively coupled RTWOs. Two magnetically coupled RTWOs are required to reduce the operating frequency within a range that the phase-hopping divider logic can handle, while maintaining good phase-noise performance and symmetry. The feedback path includes a programmable phase-hopping divider, an integer-N divider, and an error source that can be used either as a deterministic or randomized fractional-N divider. The added programmability allows for multiple reference frequencies and the ability to move any spurs in the feedback path. With $f_{ref} = 125MHz$ and Q=24 bits, the following ratios can set f_{rtwo} to 1GHz:

{FB_DIV=8; FB_INC=0; FB_FINC=0},

{FB_DIV=7; FB_INC=8; FB_FINC=0xDB6DB6},

{FB_DIV=6; FB_INC=20; FB_FINC=0xAAAAAA},

{FB_DIV=5; FB_INC=37; FB_FINC=0x333333},

{FB_DIV=4; FB_INC=62; FB_FINC=0}.

The primary spur in the feedback path is determined by $(^{FB\_FINC}/_{2^Q}) \times f_{rtwo}$, and above roughly 1MHz, it is attenuated by the loop filter.

$$f_{rtwo} = f_{ref} \times FB\_DIV \times \frac{62 + FB\_INC + {}^{FB\_FINC}/_{2^Q}}{62} \tag{9}$$

$$f_{out} = f_{rtwo} \times \frac{62}{62 + FF\_INC} \tag{10}$$

3.3 State Machine

The *Phase FSM* in Fig. 7 updates the tap position ($x = vt$). To do this, the state machine needs to run at the RTWO frequency and overflow at a tap value of 62; a block level diagram is presented in Fig. 8. The FSM consists of an accumulator (A+B+Step), a correction term adder (A+2), and a comparator (5 input NAND gate). On each clock cycle, the FSM computes the next tap position {0-61}, and if it detects an overflow, it holds the last output value and signals a *Hold* for one RTWO clock cycle. The *Hold* signal deactivates all phase taps in the phase selector, which ensures synchronization between the FSM and re-timing logic in the phase selector[3].

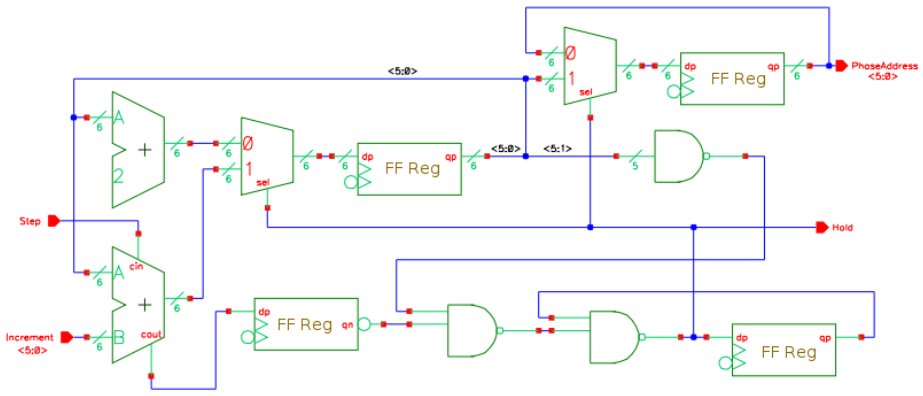


Figure 8: Phase Hopping Finite State Machine.

4 System Modeling

A full transistor level simulation of the synthesizer runs through 500ns/day in Cadence Spectre RF and $2\mu s$/day in Agilent Golden Gate, on a 4 processor Intel Xeon 3.33GHz server with 32GB of RAM. Even when the PLL is simulated with Verilog-A behavioral models, the simulation time is improved to 10-20ms/day. The issue here is that trunked radio systems use low frequency bands (60-500Hz) to send encoded data and require the carrier source to have good low frequency spur performance. To simulate such low frequency deviations, about 25ms of a transient output is needed, and this has to be repeated for several hundred frequency codes. Without access to super-computers, full system verification is impractical via any of these methods.

4.1 Direct Side Band Simulator

The premise of phase noise analysis is that a signal source $sin(2\pi f_0 t)$ is modulated by a noise component $\phi_{noise}(t)$ into an output signal $sin(2\pi f_0 t + \phi_{noise}(t))$. To extract $FFT\{\phi_{noise}(t)\}$ from the output signal, the waveform is *mixed* with a clean reference, whose noise $\phi_{ref}(t)$ should be much lower than $\phi_{noise}(t)$. The waveform is then put through a low-pass filter to eliminate the doubled frequency components (Eq. 11).

$$sin(2\pi f_0 t + \phi_{noise}(t)) \otimes cos(2\pi f_0 t + \phi_{ref}(t)) =$$

$$= sin(4\pi f_0 t + \phi_{noise}(t) + \phi_{ref}(t)) + sin(\phi_{noise}(t) + \phi_{ref}(t)) \Rightarrow$$

$$\Rightarrow \times \frac{1}{s+\tau} \Rightarrow sin(\phi_{noise}(t) + \phi_{ref}(t)) \tag{11}$$

Assuming that $\phi_{noise}(t) + \phi_{ref}(t)$ has a small amplitude, the sine can be substituted with its Taylor expansion.

$$sin(\phi_{noise}(t) + \phi_{ref}(t)) \Rightarrow \phi_{noise}(t) + \phi_{ref}(t) \Rightarrow$$

$$\Rightarrow \phi_{noise}(t); \qquad \phi_{ref}(t) \ll \phi_{noise}(t)$$

The noisy signal source can also be represented as $sin(2\pi(f_0 + f_{noise}(t)) \times t) \approx sin\left(\frac{2\pi t}{\tau_0 + \tau_{noise}(t)}\right), \quad f_0 \gg \|f_{noise}(t)\|$. With this approximation, it is possible to extract phase noise information from cycle-to-cycle time. The normalized FFT of a series of periods will produce a power spectrum analogous to $FFT\{1/(\tau_0+\tau_{noise}(t))\} \sim FFT\{\phi_{noise}(t)\}$. To overcome the simulation hurdles, I wrote a behavioral simulator that essentially bypasses several steps in traditional side band (phase noise) analysis. With a behavioral model very similar to the one used in VerilogA simulations, the computation of a single period can be drastically reduced to about 100 arithmetic operations. Through this method, 100ms of transient output (at 1GHz) can be simulated in about 10 seconds and using FFTW v3.2[8], the Fourier transform takes an additional 10 seconds of computer time. Currently the simulator accounts for timing variations between each phase and the poly-phase divider output. Work continues on including the phase noise of the RTWO, and dividers into the behavioral models.

5 Future Development

This synthesizer system contains several novel ideas among which are the phase-hopping division technique and the two magnetically coupled, injection locked RTWOs. I have completed and sent out for fabrication two test chips to measure the benefits of that RTWO design, the details of which are proprietary. In the first stages of prototyping the system was designed and simulated for the IBM 7RF $0.18\mu m$ CMOS process. For the actual system fabrication, I am redesigning the synthesizer for the IBM 7WL $0.18\mu m$ Bi-CMOS process, in which the RTWO frequency will be doubled to 2GHz. That iteration will also include circuitry to compensate for variations in the phase-to-output propagation delays.

[8]Fastest Fourier Transform in the West, is a cross platform FFT library out of MIT <http://fftw.org>.

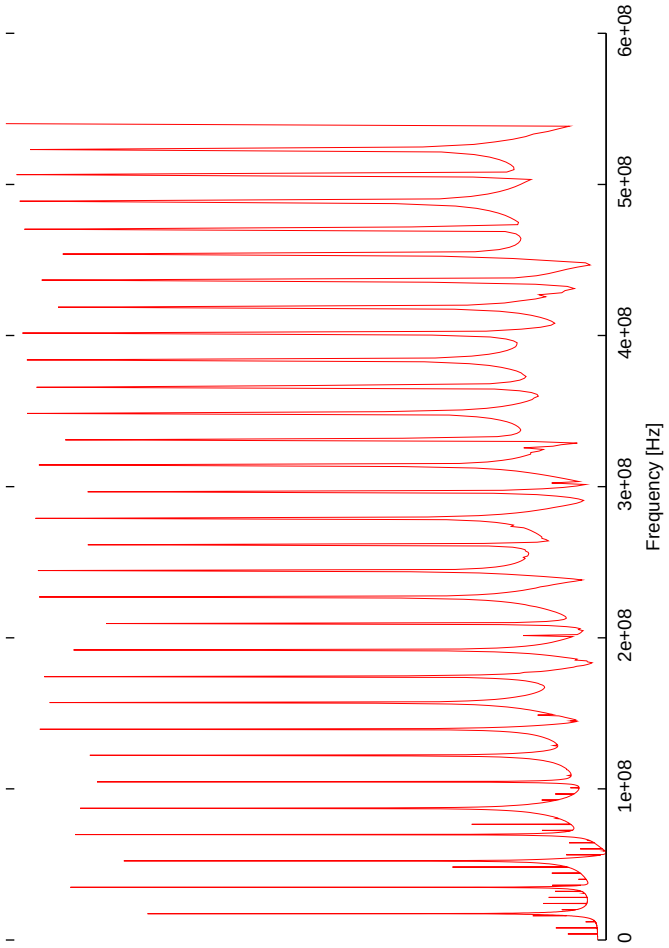


Figure 9: Side band spurs generated by random and systematic variations in propagation delays.

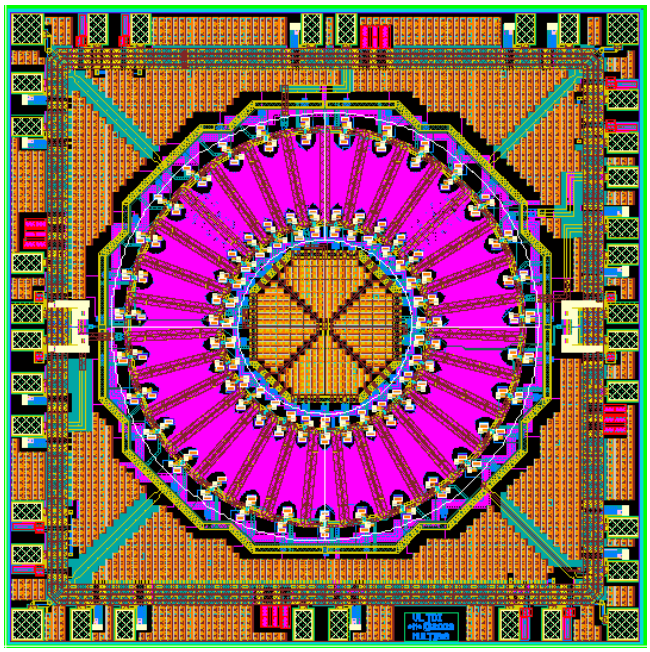


Figure 10: Die plot of one of the test chips.

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